The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

Bipolar Microcomputer Components Data Book

for

Design Engineers

JANUARY 1977

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INCORPORATED

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$2.95
(In U.S.A.)

Bipolar Microcomputer Components Data Book

for Design Engineers

First Edition

TEXAS INSTRUMENTS
INCORPORATED

LCC-4270

Printed in U.S.A.

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BIPOLAR MICROCOMPUTER COMPONENTS
DATA BOOK

This data book describes a series of high complexity bipolar digital building blocks designed specifically for implementing high performance computer or controller systems. The series offers a system designer the maximum flexibility for achieving cost-effective hardware designs from dedicated, highly specialized unique systems with tailored instructions to general-purpose computers capable of emulating existing machine instructions, or programs, without loss of software investment.

In addition to a choice between the high-performance Schottky† TTL 4-bit slice processor element, the unique performance flexibility of an I^2L 4-bit slice processor element, or a 16-bit computer central processing unit (CPU), the system designer can pick from a full family of Schottky TTL memories (RAMs, PROMs and ROMs), and state-of-the-art support functions needed to meet all control and interface requirements.

The SN54S/74S481, with a clock cycle time of 100 ns, is the industry's highest complexity Schottky TTL processor element, and the only bipolar micro/nanoprogrammable element featuring automatically sequenced iterative multiply and divide and cyclical-redundancy algorithms.

The SBP0400A and the SBP0401A, integrated injection logic (I^2L) bit slices with complete TTL/MOS compatibility, can operate at a constant speed-power product over a wide range of supply current therein offering an unmatched level of performance flexibility.

The SBP9900 microprocessor, a ruggedized monolithic parallel 16-bit (I^2L) central processing unit (CPU), combines an advanced memory-to-memory architecture, a powerful minicomputer instruction set, user-programmable speed/power performance with the simplicity of a single power supply and static logic with a single phase clock to thrust its capabilities beyond those of existing microprocessors.

The family of high-performance Schottky TTL memories offers a wide variety of organizations providing efficient solutions for virtually any size microcontrol or program memory.

System control is simplified to a very low package count with the expandable SN54S/74S482 4-bit slice controller performing next-address generation functions coupled with system status decoding performed by the industry's most versatile field-programmable logic arrays, the SN54S/74S330/'S331.

A number of advanced high-complexity I/O and interface circuits have been added to the series. Most of these I/O and interface functions as well as a number of the other processor support functions are offered in space saving 20-pin packages which reduce package count and enhance system density.

Although this volume offers design and specification data only for bipolar computer components, complete technical data for any TI semiconductor/component product are available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to: Marketing and Information Services, Texas Instruments Incorporated, P. O. Box 5012, MS 308, Dallas, Texas 75222.

We sincerely hope you will find the Bipolar Microcomputer Components Data Book a meaningful addition to your technical library.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

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NOTICE

Some products described in this document are in the developmental stage, and Texas Instruments reserves the right to change these specifications in any manner, without notice.

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†Not recommended for new designs. For data sheets, see *The Semiconductor Memory Data Book for Design Engineers*. For new designs, refer to section 4 of this manual for TI's advanced Schottky PROM and RAM families.

GLOSSARY
TTL TERMS AND DEFINITIONS

INTRODUCTION

This glossary consists of two parts: (1) general concepts for digital circuits including types of bipolar memories, and (2) operating conditions and characteristics (including letter symbols). The terms, symbols, abbreviations, and definitions used with memory integrated circuits have not, as yet, been standardized. All are currently under consideration by the EIA/JEDEC (Electronic Industries Association) and the IEC (International Electrotechnical Commission). The following are as consistent with the past and future work of these organizations as is possible to anticipate at this time.

PART I – GENERAL CONCEPTS INCLUDING TYPES OF BIPOLAR MEMORIES

Chip-Enable Input

A control input that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in a reduced-power standby mode.
NOTE: See "chip-select input".

Chip-Select Input

A gating input that when inactive prevents input or output of data to or from an integrated circuit.
NOTE. See "chip-enable input".

Dynamic (Read/Write) Memory

A read/write memory in which the cells require the repetitive application of control signals in order to retain stored data.
NOTES. 1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

First-In First-Out (FIFO) Memory

A memory from which data bytes or words can be read in the same order, but not necessarily at the same rate, as that of the data entry.

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration, LSI

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Mask-Programmed Read-Only Memory

A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Medium-Scale Integration, MSI

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Memory Cell

The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Memory Integrated Circuit

An integrated circuit consisting of memory cells and usually including associated circuits such as those for address selection, amplifiers, etc.

Output-Enable Input

A gating input that when active permits the integrated circuit to output data and when inactive causes the integrated circuit output(s) to be at a high impedance (off).

Programmable Read-Only Memory (PROM)

A read-only memory that after being manufactured can have the data content of each memory cell altered once only.

Random-Access Memory (RAM)

A memory that permits access to any of its address locations in any desired sequence with similar access time for each location.
NOTE: The term RAM, as commonly used, denotes a read/write memory.

Read-Only Memory (ROM)

A memory in which the contents are not intended to be altered during normal operation.
NOTE: Unless otherwise qualified, the term "read-only memory" implies that the content is unalterable and defined by construction.

Read/Write Memory

A memory in which each cell may be selected by applying appropriate electronic input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electronic input signals.

Small-Scale Integration, SSI

Integrated circuits of less complexity than medium-scale integration (MSI).

Very-Large-Scale Integration, VLSI

A concept whereby a complete system function is fabricated as a single microcircuit. In this context, a system, whether digital or linear, is considered to be one that contains 1000 or more gates or circuitry of similar complexity.

Volatile Memory

A memory the data content of which is lost when power is removed.

PART II – OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

The symbols for quantities involving time use upper and lower case letters according to the following historically evolved principles:

a. Time itself, is always represented by a lower case t.

b. Subscripts are lower case when one or more letters represent single words, e.g., d for delay, su for setup, rd for read, wr for write.

c. Multiple subscripts are upper case when each letter stands for a different word, e.g., SR for sense recovery and PLH for propagation delay from low to high.

Access Time (of a memory)

The time between the application of a specified input pulse during a read cycle and the availability of valid data signals at an output.

Example symbology:

$t_{a(ad)}$	Access time from address
$t_{a(E)}$	Access time from chip enable
$t_{a(S)}$	Access time from chip select

Clock Frequency

Maximum clock frequency, f_{max}
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transistions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

Current

High-level input current, I_{IH}
The current into* an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}
The current into* an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state output current, $I_{O(off)}$
The current flowing into* an output with input conditions applied that according to the product specification will cause the output switching element to be in the off state.
Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits.

*Current out of a terminal is given as a negative value.

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Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}
The current into* the V_{CC} supply terminal of an integrated circuit.

Cycle Time

Read cycle time, $t_{c(rd)}$ (see note)
The time interval between the start and end of a read cycle.

Read-write cycle time, $t_{c(rd,wr)}$ (see note)
The time interval between the start of a cycle in which the memory is read and new data are entered, and the end of that cycle.

Write cycle time, $t_{c(wr)}$ (see note)
The time interval between the start and end of a write cycle.

NOTE: The read, read-write, or write cycle time is the actual interval between two impulses and may be insufficient for the completion of operations within the memory. A minimum value is specified that is the shortest time in which the memory will perform its read and/or write function correctly.

Hold Time

Hold time, t_h
The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

*Current out of a terminal is given as a negative value.

Output disable time (of a three-state output) from high or low level, t_{PXZ}
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Propagation Time

Propagation delay time, t_{PD}
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

Pulse Width

Pulse width, t_w
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

$t_{w(clr)}$	Clear pulse width
$t_{w(wr)}$	Write pulse width

Recovery Time

Sense Recovery time, t_{SR}
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

Release Time

Release time, $t_{release}$
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.
Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

Setup Time

Setup time, t_{su}
The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.
NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

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Transition Time

Transition time, low-to-high-level, t_{TLH}
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

Transition time, high-to-low-level, t_{THL}
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

Voltage

High-level input voltage, V_{IH}
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Input clamp voltage, V_{IK}
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Negative-going threshold voltage, V_{T-}
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

Off-state output voltage, $V_{O(off)}$
The voltage at an output terminal with input conditions applied that according to the product specification will cause the output switching element to be in the off state.
Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

On-state output voltage, $V_{O(on)}$
The voltage at an output terminal with input conditions applied that according to the product specification will cause the output switching element to be in the on state.
Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

Positive-going threshold voltage, V_{T+}
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
a . . h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\bar{Q}_0$	=	complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎴	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

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SN54S481
SN74S481
4-Bit-Slice Schottky Processor Elements Data Manual

NOVEMBER 1976

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1. INTRODUCTION

1.1 ARCHITECTURAL FEATURES

The SN54S481, SN74S481 are Schottky TTL 4-bit expandable parallel binary micro/macroprogrammable processor element building blocks designed specifically for implementing high-performance digital computers/controllers. The 'S481, with its ability to efficiently emulate existing systems, can be used to upgrade hardware performance with full compatibility to protect the software investments.

Designed with full parallel dual input/output ports, the memory-to-memory architecture of the 'S481 provides a new dimension in interrupt processing or program context switching flexibilities. Its static bipolar logic performs each microinstruction within a single 100 ns clock cycle.

Primary among the 'S481 architectural features are:

- Microprogrammable, bit-slice design is expandable in 4-bit multiples
- Full parallel dual input/output ports for use in advanced memory-to-memory architecture
- Full-function ALU with carry look-ahead, magnitude, and overflow decision capabilities
- Double-length accumulator with full shifting capability and sign-bit handling
- Dual memory address generators on-chip.

1.2 OPERATIONAL FEATURES

The functional capabilities, characterized by the 24,780 unique operations of the 'S481, coupled with its macroprogrammable multiply and divide algorithms, make the 'S481 particularly attractive for implementing advanced high performance computers and controllers.

In addition to the full parallel data bus structure, the 'S481 architecture also features asynchronous access to data routing and counter updating controls which, when combined with the most versatile instruction set available (see operational description) maximizes flexibility, efficiency, and performance. Simultaneous compound operations in the form of an ALU function with shift, plus destination selection with address/iteration updating, plus address *and* present data to memory can be accomplished in a single microcycle. Some other operational features are:

- Simultaneous one-clock compound operations with status can reduce microcycles and improve throughput
- Pre-programmed multiply, divide, and CRG algorithms
- Performs 16-bit by 16-bit double-precision divide in less than 3 microseconds
- Double length accumulator with full bidirectional single/double precision arithmetic/logical/circulate shift capabilities include sign protection
- Full-micro-operational control is provided for programming: address updating, data and address source selection, and direct transfer of data to working register or working memory
- Relative position control defines bit-slice rank and sign handling in N-bit applications.

1.3 MECHANICAL FEATURES

The 'S481 is supplied in a high-density 48-pin package with the qud pin rows formed on 600- and 800-mil centers. Within each of the four rows pin spacing is 100-mils, center-to-center. See mechanical data for detailed dimensions.

DESIGN GOAL
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

TABLE 1
FUNCTIONAL DESCRIPTIONS

PIN NUMBER	PIN NAME	PIN FUNCTION	INPUT, OUTPUT, OR INPUT/OUTPUT
46, 47 1, 2	BI/O0, BI/O1 BI/O2, BI/O3	4-bit parallel data input port to the B latch, or 4-bit parallel data output for the Σ-bus when not being used as an input.	Inputs/Outputs
6, 5 4, 3	AI0, AI1 AI2, AI3	4-bit parallel data input port to the A latch and WR	Inputs
7, 8 9, 10 17, 14 13, 11 15, 16	OP0, OP1 OP2, OP3 OP4, OP5 OP6, OP7 OP8, OP9	OP0 through OP9 serve as a 10-bit parallel operation-select input to the micro-decode logic array. In the most-significant position, OP8 and OP9 additionally serve as open-collector outputs during multiply and divide algorithms. In the least-significant position, OP9 serves as an open-collector output during the CRC algorithm.	Inputs
12	V_{CC}	Single 5-volt power-supply terminal.	Supply Voltage Pin
18	$\overline{CIN}$	Receives low-active ripple carry input data.	Input
19	POS	Directs internal and input-output end-conditions required to define the relative position of each bit-slice when N-SN74S481's are cascaded to implement N×4-bit word lengths. When biased at 2.4 volts, the package operates as the least-significant (LSP) slice; when grounded, it functions as an intermediate (IP) slice; and when high, 5 volts, it functions as the most-significant (MSP) slice.	Input
20	Y/AG	In least-significant and intermediate positions outputs arithmetic carry generate (Y) for use with look-ahead. In most-significant position outputs true arithmetically-greater-than signal.	Output
21	X/LG	In least-significant and intermediate positions outputs arithmetic carry propagate (X) for use with look-ahead. In most-significant position outputs true logically-greater-than signal.	Output
22	$\overline{COUT}$	Outputs low-active ripple carry data.	Output
23	EQ	Outputs true (active-high) equality of Σ bus equals zero for each 4-bit slice. The open-collector output permits wire-AND to achieve N×4-bit equality output.	Open-Collector-Output
24	$\overline{LD\ WR}$	When low, data applied at the AI port coincident with the ↑ clock transition is loaded into the WR.	Input
26 25	WRRT, WRLFT	Working register and Σ-bus shift interconnectivity pins. WRRT receives left-shift and outputs right-shift (true) data. WRLFT receives right-shift and outputs left-shift (true) data. Shift can be single-precision, double-precision, signed or unsigned.	Bidirectional I/O
28 27	XWRRT, XWRLFT	Extended working register shift interconnectivity pins. XWRRT receives left-shift and outputs right-shift (true) data. XWRLFT receives right-shift and outputs left-shift (true) data. Shift can be single-precision, double-precision, signed or unsigned.	Bidirectional I/O
29 30	D0 D1	Selects one of three DOP sources (WR, XWR, or Σ-bus) or places the DOP outputs in a high-impedance state.	Inputs
34 33 32 31	DOP0 DOP1 DOP2 DOP3	4-bit parallel, data-out port. DOP0 is LSB.	3-state outputs
35	$\overline{INCMC}$	When low, enables the MC to increment as directed by $\overline{CCI}$ on the next ↑ clock transition. When high, inhibits MC to hold mode. As $\overline{CCO}$ is common to MC and PC, the MC should be inhibited when PC is enabled.	Input
36	GND	Common or ground terminal for the supply voltage	
37	$\overline{CCO}$/OV	In least-significant and intermediate positions a low-level output indicates that either the PC or MC is at maximum count. As $\overline{CCO}$ is common for both PC and MC ambiguous carry can be avoided if one or both counters is/are disabled by the $\overline{INCPC}$ and/or $\overline{INCMC}$ inputs. In the most-significant position, a high-level output, depending on the operation selected, indicates that the WR, XWR, or ALU will overflow (OV) on the next clock.	Output

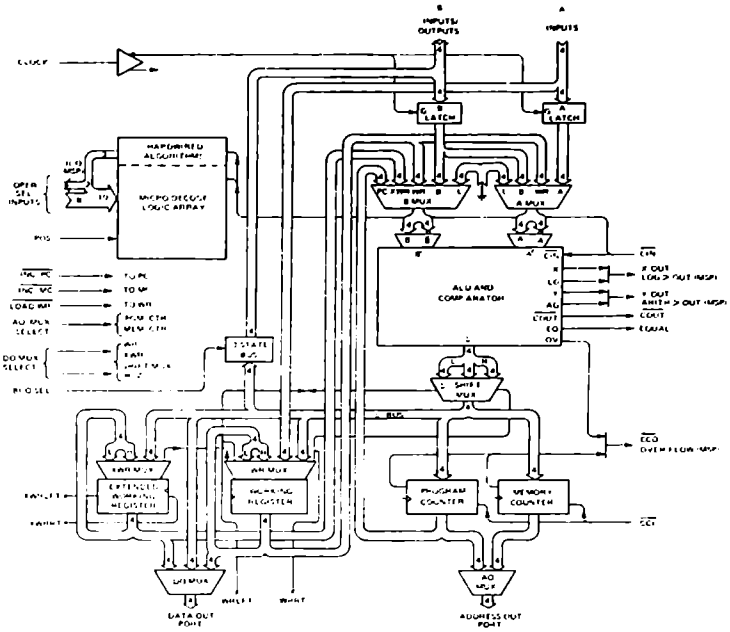


FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM

TABLE 1 (Continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	INPUT, OUTPUT, OR INPUT/OUTPUT
38, 39 40, 41	AOP0, AOP1 AOP2, AOP3	4-bit parallel address-out port.	Outputs
42	A0	Selects one of two AOP sources (PC or MC).	Input
43	$\overline{INCPC}$	When low, enables the PC to increment as directed by $\overline{CCI}$ on the next ↑ clock transition. When high, inhibits PC to hold mode. As $\overline{CCO}$ is common to PC and MC, the PC should be inhibited when MC is enabled.	Input
44	$\overline{CCI}$	In least-significant position, a low input directs enabled PC or enabled MC to increment by one on next ↑ clock transition. In the LSP, a high directs enabled PC or enabled MC to increment by 2. In other positions, a low is a carry input and a high inhibits the counter.	Input
45	CK	When high, enables the transparency of A and B input latches. When low, latches A and B input data. Clocks synchronous registers and counters on the positive transition.	Input
48	BI/O SEL	When low, enables BI/O to output Σ-bus data. When high, the BI/O output drivers are placed in a high-impedance state permitting BI/O to be used as data inputs.	Input

2. DETAILED FUNCTIONAL DESCRIPTIONS

2.1 MICRO-DECODING LOGIC ARRAY

The micro-decoding logic array is a dedicated 11 input PLA decoding 73 product terms to generate 24 control lines needed to implement the 14 operation forms. The eleven inputs consist of the ten operation select lines (OP0 through OP9) and the ALU carry input. The carry input, utilized as an additional operation select line during operation forms not performing arithmetic functions, maximizes system pin efficiency and functional density.

In an expanded word-length system (two or more 'S481's), operation select inputs 8 (OP8) and 9 (OP9) assume an input/output capability in the most-significant or least-significant package as a result of the position control and the type of operation being performed. During microprogrammable operation forms I through IX, OP8 and OP9 function simply as another input; but, during the macroprogrammable operations of forms X through XIV one or both become an output during iterations. Table 2 summarizes by operation form the control (output) package and the operation lines which are used as an output.

TABLE 2
MSP OP8 and OP9 ITERATIVE FUNCTION SUMMARY

OP. FORM	ALGORITHM	CONTROL PACKAGE	OPERATION SELECT I/O	
			OP8	OP9
I thru IX	All	None	INPUT	INPUT
X	CRC ACCUMULATION	LSP	INPUT	OUTPUT
XI	SIGNED DIVIDE	MSP	OUTPUT	OUTPUT
XII	UNSIGNED DIVIDE	MSP	INPUT	OUTPUT
XIII	UNSIGNED MULTIPLY	MSP	INPUT	OUTPUT
XIV	SIGNED MULTIPLY	MSP	OUTPUT	OUTPUT

If the macroinstructions are to be used in an expanded word length, OP8 and OP9 select lines of the MSP and the OP9 line of the LSP should be driven from either a 3-state output (which can be placed in high-impedance state) or an open-collector output (which can be wire-OR'ed with the OP select I/O lines). During an iterative function for which the OP line is designated as an open-collector output, the OP line driver should be placed in a high-impedance or off state permitting the output function to drive similar OP lines in the remaining packages.

The output state of OP8 or OP9 is a function of on-chip status decoder as enumerated in the flow diagrams illustrating the five algorithms.

2.2 RELATIVE POSITION CONTROL (POS)

The single line position control, with the ability of decoding one of three input logic states, provides each 'S481 in an expanded word length system with the capability of identifying its relative position. The relative positions, with the corresponding input logic levels are enumerated in Table 3.

TABLE 3
POSITION CONTROL FUNCTIONS

POS INPUT LOGIC LEVEL	RELATIVE POSITION
> 3.6 V	MOST-SIGNIFICANT POSITION (MSP)
1.8 V to 3 V	LEAST-SIGNIFICANT POSITION (LSP)
< 0.8 V	INTERMEDIATE POSITION (IP)

This relative position identification dictates how each 'S481 in the system handles the multi-purpose I/O accommodations and ALU sign and magnitude functions. See Table 4. Shift/Circulate interconnectivity bit transfers are explained in detail under shift/circulate transfer multiplexers.

TABLE 4
DUAL-FUNCTION LOGIC I/O PINS

PIN	MSP	IP	LSP
X/LG	LG (OUT)	X	X
Y/LG	AG (OUT)	Y	Y
$\overline{CCO}$/OV	OVERFLOW (OUT)	$\overline{CCO}$ (OUT)	$\overline{CCO}$ (OUT)

X AND Y ARE CARRY LOOK-AHEAD FUNCTIONS

2.3 CLOCK

The clock synchronizes the entry or change of data in the 'S481 registers and counters, and it controls the status of the A and B input latches. A typical clock cycle is illustrated in Figure 2. The low-to-high transition of the clock input is the clocking edge for any combination of either the working register, extended working register, flag flip-flops, and the program counter or the memory counter activated by the resident operation. During the low-level portion of the clock input, both input latches are latched ensuring data stability at the positive clock transition. After the clock has gone to a high level, the input latches are placed in a transparent mode to accept the next set of input data.

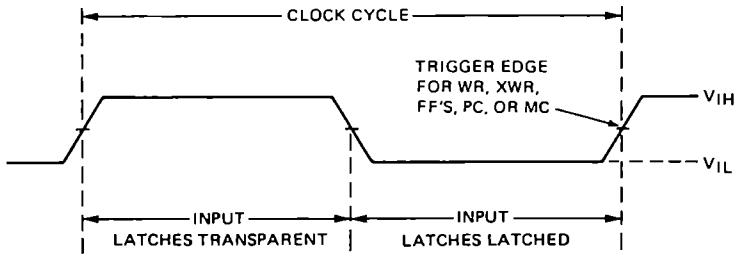


FIGURE 2 – CLOCK CYCLE

2.4 LATCHED DATA INPUT PORTS

The SN54S/74S481 features dual input ports combined with data flow paths which are designed specifically to reduce the number of system clock cycles needed to enter operands and/or data. Both the A and B input ports are latched, eliminating the need for external registers, to simplify interfacing directly with system data bus paths.

The A input port data is made available to both the input latch and the working register which allows A data to be loaded into the working register directly.

The B port is configured to serve as an input/output data path providing the capability to:

a. Input data to the B latch
b. Output sum-bus data.

This I/O port is designed specifically to simplify implementation of data transfers to the external working memory.

Both the A and B latches are transparent when the 'S481 clock input is high. Data applied at the A and B inputs should be stable anytime prior to or at least coincident with the falling edge of the clock input (see Figure 3). After the clock falling edge, the data inputs should be held steady for $t_{hold(data)}$ or longer to facilitate the on-chip clock buffers to latch the data.

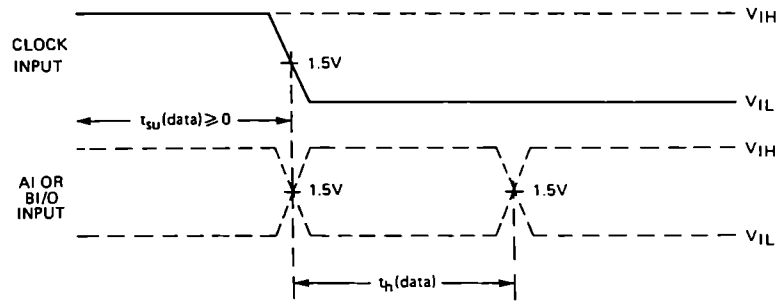


FIGURE 3 – INPUT LATCHES SETUP/HOLD TIMES

The A input port latch data is routed to the A input multiplexers, and the B input port latch data is sourced to both the A and B input multiplexers.

2.5 A AND B OPERAND SOURCES

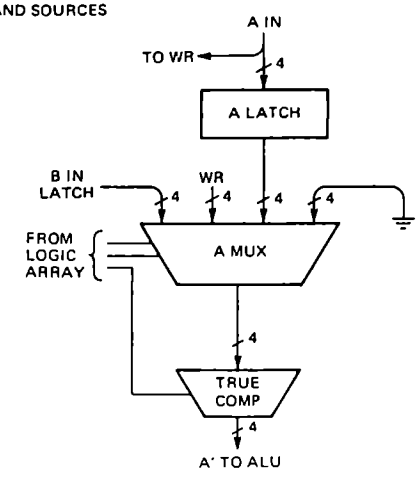
The A and B input multiplexers source the ALU A' and B' ports through true/complement conditional inverter circuits. Data routing for each, illustrated and listed in Figure 4, provides the ALU with access to the true or complement of:

ALU A' PORT	ALU B' PORT
1. A input latch	1 B input latch
2. B input latch	2. Sum bus
3. Working Register	3 Working register
4. Low logic level inputs (force zeros)	4. Extended working register
	5. Program counter
	6. Low logic level inputs (force zeros)

The A and B multiplexers and true complement circuits, under control of the resident operation code, are selectable at the microprogram level. The number of A or B multiplexer sources available depend upon the specific operation being performed by the 'S481. Operation form descriptions contain detailed microprogramming.

The A and B input multiplexers, with selectable true and complement operand sources, maximizes the processing power of the 'S481 by minimizing the active components needed to achieve both the simple but highly flexible data routing tasks and full ALU capabilities.

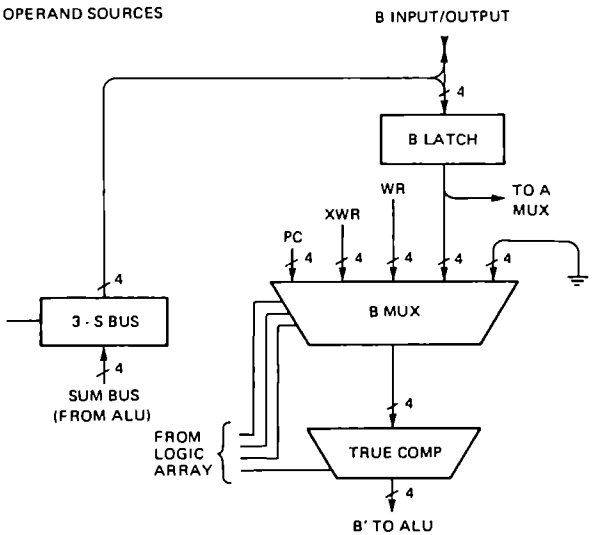
A OPERAND SOURCES



A INPUT SELECTIONS

A IN → A'
$\overline{\text{A IN}}$ → A'
LOGIC ONE'S → A'
LOGIC ZERO'S → A'
B IN → A'
$\overline{\text{B IN}}$ → A'
WR → A'
$\overline{\text{WR}}$ → A'

B OPERAND SOURCES



B INPUT/OUTPUT SELECTIONS

B IN → B'
$\overline{\text{B IN}}$ → B'
LOGIC ONE'S → B'
LOGIC ZERO'S → B'
(B IN) · (WR) → B'
$\overline{\text{(B IN) · (WR)}}$ → B'
WR → B'
$\overline{\text{WR}}$ → B'
(B IN) · (XWR) → B'
$\overline{\text{(B IN) · (XWR)}}$ → B'
XWR → B'
$\overline{\text{XWR}}$ → B'
(B IN) · (PC) → B'
$\overline{\text{(B IN) · (PC)}}$ → B'
PC → B'
$\overline{\text{PC}}$ → B'

FIGURE 4 – ALU OPERAND SOURCES

2.6 ARITHMETIC/LOGIC UNIT (ALU)

The 4-bit, parallel, binary arithmetic/logic unit provides the arithmetic/Boolean operand combination/modification mechanism including magnitude and overflow status. The ALU performs, as directed by the resident operation form, one of four basic functions which, when combined with the operand selections at the A and B multiplexers, extends the arithmetic/logic capabilities to that of a full 16-function ALU.

When compared to other bit-slice processor elements, unique to the 'S481 arithmetic architecture are the parallel input ports and fully microprogrammable symmetry for all ALU functions within the selections of the A and B input multiplexers.

Logical and arithmetic operation forms for the 'S481 are shown in Table 5. The full functional power of the 'S481 can be visualized only if it is understood that although both ALU's have parallel A and B input ports, the 'S481 architecture not only provides access to multiple sources but has the capability to route true or complement of any source to the A and B ALU port. This means that for a subtract operation, the subtrahend may be either an A or B input. In addition to maximizing data routing capabilities of the 'S481 at minimum logic/gate levels, this architecture permits fully symmetrical operations to be performed on the A or B sources within the selections offered by these 'S481 arithmetic/logical operation forms.

TABLE 5
'S481 ALU AND LOGIC FUNCTIONS

DATA INPUT		TWO'S COMPLEMENT INTEGER ARITHMETIC OP'S		LOGICAL OP'S (FORM VIII) $\overline{CIN}$ = H OR L		
A PORT	B PORT	$\overline{CIN}$ = L	$\overline{CIN}$ = H	OR	NOR	EX-NOR
ZEROS	ZEROS	1	0	ZEROS	ONES	ONES
ZEROS	ONES	0	MINUS 1	ONES	ZEROS	ZEROS
ONES	ZEROS	0	MINUS 1	ONES	ZEROS	ZEROS
ONES	ONES	MINUS 1	MINUS 2	ONES	ZEROS	ONES
A	ZEROS	A PLUS 1	A	A	$\overline{A}$	$\overline{A}$
A	ONES	A	A MINUS 1	ONES	ZEROS	A
$\overline{A}$	ZEROS	MINUS A	MINUS A MINUS 1	$\overline{A}$	A	A
$\overline{A}$	ONES	MINUS A MINUS 1	MINUS A MINUS 2	ONES	ZEROS	$\overline{A}$
ZEROS	B	B PLUS 1	B	B	$\overline{B}$	$\overline{B}$
ONES	B	B	B MINUS 1	ONES	ZEROS	B
ZEROS	$\overline{B}$	MINUS B	MINUS B MINUS 1	$\overline{B}$	B	B
ONES	$\overline{B}$	MINUS B MINUS 1	MINUS B MINUS 2	ONES	ZEROS	$\overline{B}$
A	B	A PLUS B PLUS 1	A PLUS B	A + B	$\overline{A} \cdot \overline{B}$	$\overline{A \oplus B}$
A	$\overline{B}$	A MINUS B	A MINUS B MINUS 1	A + $\overline{B}$	$\overline{A} \cdot B$	A ⊕ B
$\overline{A}$	B	B MINUS A	B MINUS A MINUS 1	$\overline{A}$ + B	A · $\overline{B}$	A ⊕ B
$\overline{A}$	$\overline{B}$	MINUS A MINUS B MINUS 1	MINUS A MINUS B MINUS 2	$\overline{A}$ + B	A · B	$\overline{A \oplus B}$

Some unique one-clock arithmetic/iterative capabilities of the 'S481 are listed in Table 6.

TABLE 6
EXTENDED ALU FUNCTIONS OF 'S481

FORM NO.	FUNCTION
I	A (ALU) B · WR A (ALU) B · XWR A (ALU) B · PC
II	A (ALU) B DOUBLE-PRECISION SHIFTED LOGICAL LEFT OR RIGHT
III	A (ALU) B SINGLE-PRECISION SHIFTED LOGICAL OR ARITHMETIC LEFT OR RIGHT

Table 5 also indicates the 16 logical combinations of two Boolean variables which are selectable for the OR, NOR, and exclusive-NOR functions. Full symmetry of the ALU and the ability to select the complement of input data extends the logic functions for performance of:

a. NAND
b. AND
c. Exclusive-OR
d. Mixed combinations of each
e. Transfer functions for true or inverted data
f. All ones or all zeros.

2.7 ALU MAGNITUDE AND CARRY FUNCTIONS

The 'S481 ALU is fully decoded on chip to generate three magnitude outputs (status lines) and both ripple and look-ahead carry functions. The magnitude outputs and their status indications are as follows:

2.7.1 Equal (EQ, See Figure 5)

The results of the resident ALU operation are compared at the sum-bus for all bits high during subtract and left-shift arithmetic operations, or for all bits low during other operations.

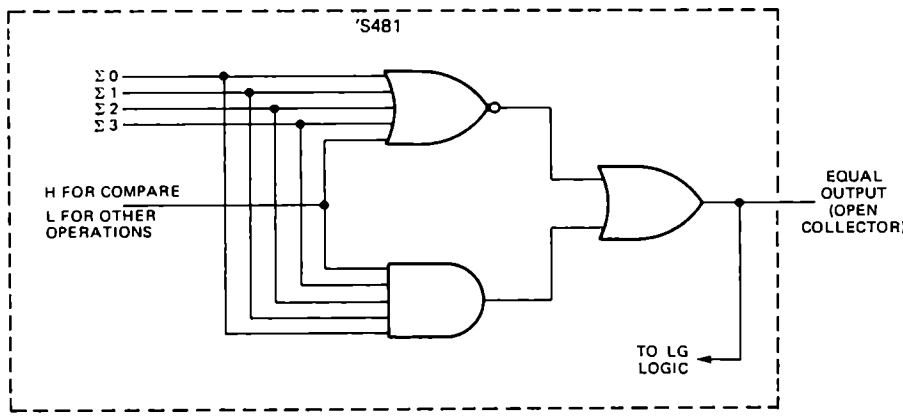


FIGURE 5 – EQUAL OUTPUT

2.7.2 Logically-Greater Than (LG, See Figure 6)

In the most-significant package (MSP) the X look-ahead function from the ALU is inhibited and the logically-greater-than (LG) output is enabled. See Figure 6. The MSP LG output is active during arithmetic and shift operation forms to provide a status indication that can be used when it is desirable to compare two unsigned integer numbers. The specific status for each operation form is listed in Table 7.

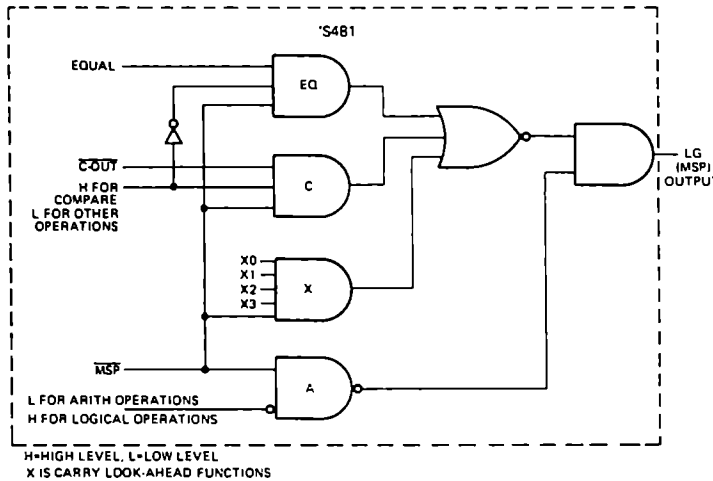


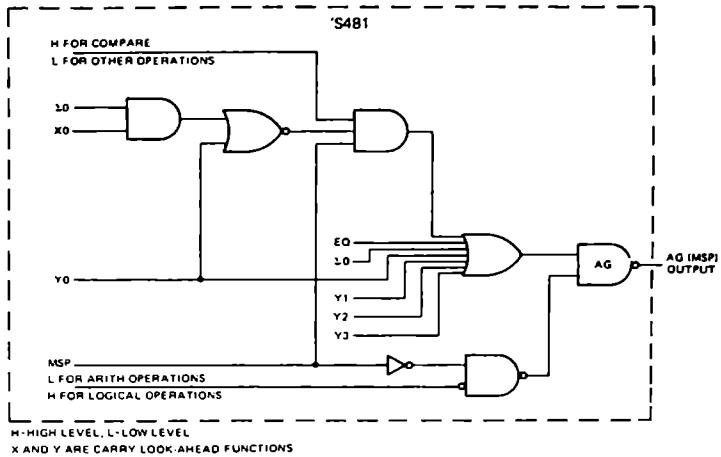
FIGURE 6 – MSP LOGICALLY-GREATER-THAN (LG) OUTPUT

TABLE 7
MSP LOGICALLY-GREATER-THAN (LG) OUTPUT

OP FORM	TYPE OF OP	LG = H INDICATES
I or II (ARITH)	ALL	Σ-BUS ≠ ZERO (EQ = L)
III (ARITH WITH SHIFT)	LSL, RSL	Σ-BUS ≠ ZERO (EQ = L)
	LSA or RSA	ADDER C-OUT
IV, V, or VI (SHIFTS)	ALL	Al ≠ ZERO (EQ = L)
VII (COMPARE)	A > B	A IS LG THAN B
	B > A	B IS LG THAN A
VIII (LOGICAL)	ALL	Σ-BUS ≠ ZERO (EQ = L)
IX (NO OP)	ZERO Σ-BUS	LG = L (EQ = H)
X THRU XIV	HARDWIRED ALGORITHMS	SEE OPERATION FORM DESCRIPTION

2.7.3 Arithmetically-Greater Than (AG, See Figure 7)

In the most-significant package (MSP) the Y look-ahead function from the ALU is inhibited and the arithmetically-greater-than (AG) output is enabled. The MSP AG output is active during arithmetic and shift operation forms to provide a status indication that can be used when it is desirable to compare two signed integer numbers. The specific status for each operation form is listed in Table 8.



H-HIGH LEVEL, L-LOW LEVEL
X AND Y ARE CARRY LOOK-AHEAD FUNCTIONS

FIGURE 7 – MSP ARITHMETICALLY-GREATER-THAN (AG) OUTPUT

TABLE 8
ALU CARRY AND MSP ARITHMETICALLY-GREATER-THAN (AG) OUTPUTS

OPERATION FORM	LSP AND IP				MSP			
	X	Y	EQ	$\overline{C\text{-}OUT}$	LG	AG	EQ	$\overline{C\text{-}OUT}$
LOGICAL OPERATIONS	L	H	Σ-BUS = 0	$\overline{C\text{-}IN}$	Σ-BUS ≠ 0	Σ-BUS > 0	Σ-BUS = 0	$\overline{C\text{-}IN}$
ARITHMETIC OPERATIONS:								
SUBTRACTION WITH LSA OR RSA	X	Y	Σ-BUS = 1's	$\overline{C\text{-}OUT}$	ADDER C-OUT	MINUEND + C-IN IS AG THAN SUBTRAHEND	Σ-BUS = 1's	$\overline{C\text{-}OUT}$
ALL OTHER ARITHMETIC	X	Y	Σ BUS = 0	$\overline{C\text{-}OUT}$	Σ-BUS ≠ 0	Σ-BUS > 0	Σ-BUS = 0	$\overline{C\text{-}OUT}$

X and Y are carry look ahead functions.

2.8 OPERAND OVERFLOW

In the most-significant package (MSP) the counter-carry output ($\overline{CCO}$) function from the program/memory counter is inhibited and the overflow (OV) output is enabled. The MSP OV output is active during arithmetic and shift operation forms to provide a status indication that the result of the operation cannot be correctly represented with the number of bit positions available. When the OV output goes high, it indicates that the next clock will:

a. During arithmetic operations, cause the ALU to overflow.
b. During left-shift arithmetic operations, cause the shifted register to overflow.

Table 9 enumerates the specific indicators generated.

TABLE 9
MSP OVERFLOW (OV) OUTPUT

OP FORM	TYPE OF OP	OV = H INDICATES
I or II (ARITH)	ADD or SUB	ALU OVERFLOW
III (ARITH WITH SHIFT)	LSL, RSL	ALU OVERFLOW
	RSA	OV L
	LSA	NEXT CLOCK WILL CAUSE SHIFT OVERFLOW
IV, V, or VI (SHIFTS)	LSA	NEXT CLOCK WILL CAUSE SHIFT OVERFLOW
	ALL OTHERS	OV L
VII (COMPARE)	A : B	UNDEFINED
	B : A	UNDEFINED
VIII (LOGICAL)	ALL	OV L
IX (NO OP)	ZERO Σ-BUS	OV L
X THRU XIV	HARDWIRED ALGORITHMS	SEE OPERATION FORM DESCRIPTIONS

H = high level, L = low level

2.9 SUM' BUS MULTIPLEXER

The sum'-bus multiplexer, sourced by the ALU, provides a means for accomplishing a shift operation on the ALU operand without affecting the contents of WR, XWR, PC or MC (See Figure 8). Functionally, this multiplexer can be used to:

a. Shift the operand left or right (one bit position) arithmetic, logical, or circulate
b. Pass the operand without shift to the Σ' bus.

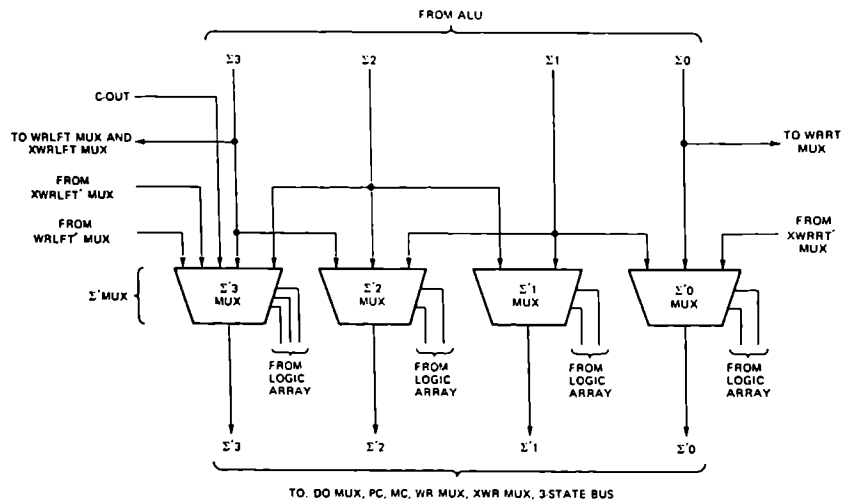


FIGURE 8 – SUM BUS MULTIPLEXER

Full sign protection and fill-in is provided in the MSP and LSP under control of the relative position inputs.

Information on the Σ' bus can be accessed during some operations through the 3-state Σ' bus control buffer at the B input/output port.

The parallel data input ports and the I/O capability of the B port, combined with the Σ-bus access, provides considerable flexibility for performing simple shifts or combinations of operation-and-shift on data or operands resident in the external working memory locations.

2.10 B-INPUT/OUTPUT CONTROL

The B-input/output port is isolated from the sum' bus by a 3-state control buffer when the buffer outputs are at a high-impedance. Enabling the buffer routes the sum' bus data to the B-port. The low-current inputs of the B port latch minimizes loading effects, and the buffers can source 6.5 mA or sink 10 mA of drive current in the output mode. During the output mode, the 'bus data can be latched in the B input latch. Enabling or disabling is accomplished by the I/O control input. See Table 10 and Figure 9.

TABLE 10
B-INPUT/OUTPUT CONTROL

I/O CONTROL	I/O BUFFER OUTPUT
L	SUM' BUS DATA
H	HIGH-IMPEDANCE

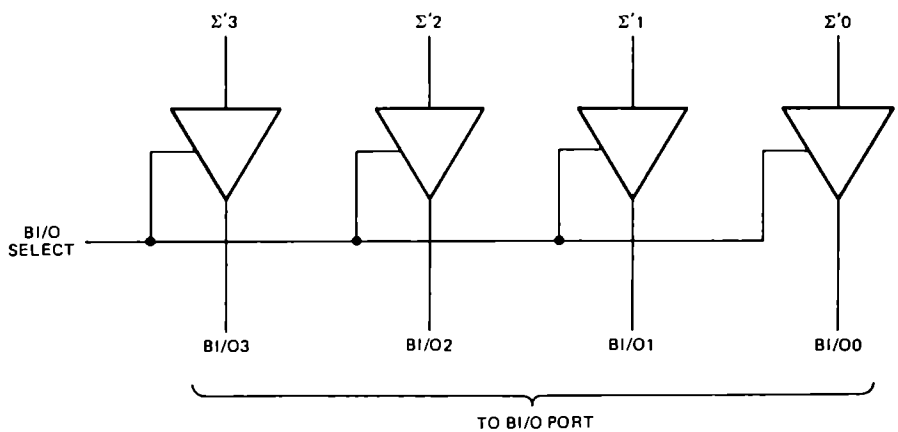


FIGURE 9 – B-INPUT/OUTPUT CONTROL

2.11 WORKING REGISTER

The working register (WR) is a 4-bit D-type register which functions as an accumulator during iterative arithmetic operations or as a temporary holding register for intermediate operands (see Figure 10). It is sourced by the WR multiplexer. Storage of setup data, under control of the resident operation forms which permit the WR to be a destination, occurs on the positive transition of the clock. WR shifting capabilities are implemented in the WR multiplexer. The working register can be selected to source the data-out port multiplexer (DO MUX), A-input multiplexer (A MUX), or B-input multiplexer (B MUX). The MSB of the WR is sourced to the WRLFT MUX, and the LSB of the WR is sourced to the WRRT MUX to facilitate expansion.

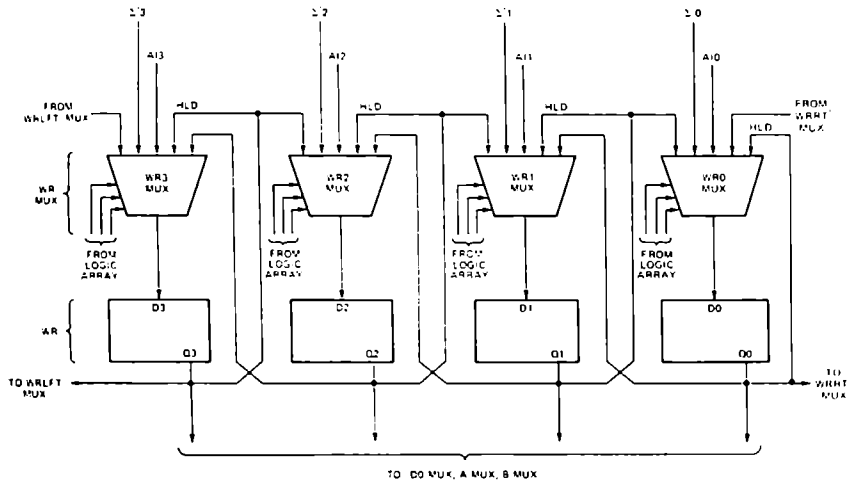


FIGURE 10 – WORKING REGISTER (WR) AND WR MULTIPLEXER

An asynchronous control line, $\overline{\text{LDWR}}$, is available to facilitate loading the working register directly from the A input port in combination with the resident micro-operation.

2.12 WORKING REGISTER MULTIPLEXER (WR MUX)

The working register multiplexer provides source selection, including the bidirectional shifting capability, for the working register. See Figure 10. Under direction of the resident operation, the WR MUX asynchronously selects either:

a. A input port for direct loading
b. Σ' bus for ALU operand results

c. Hold mode for no change
d. Shift left
e. Shift right

End conditions for both shift left and shift right operations are routed to or from WR MSB (WR3) or WRLSB (WR0) to the WRLFT/WRLFT' multiplexers or to the WRRT/WRRT' multiplexers respectively.

2.13 EXTENDED WORKING REGISTER

The extended working register (XWR) is a 4-bit D-type register which functions primarily as an extension of the working register to provide the double-precision operation capabilities needed for iterative multiply and divide routines (see Figure 11). Additionally, the storage capabilities of the XWR are available for use as another temporary holding register for intermediate operands during a number of the single-precision operation forms. It is sourced by the XWR multiplexer. Storage of setup data, under control of resident operation forms which permit the XWR to be a destination, occurs on the positive transition of the clock. XWR shifting capabilities are implemented in the XWR multiplexer. The XWR can be selected to source the data-out port multiplexer (DO MUX), B-input multiplexer (B MUX), or the XWR multiplexer (XWR MUX). The MSB of the XWR is sourced to the XWRLFT' MUX, and the LSB of the XWR is sourced to the XWRRT' MUX to facilitate expansion.

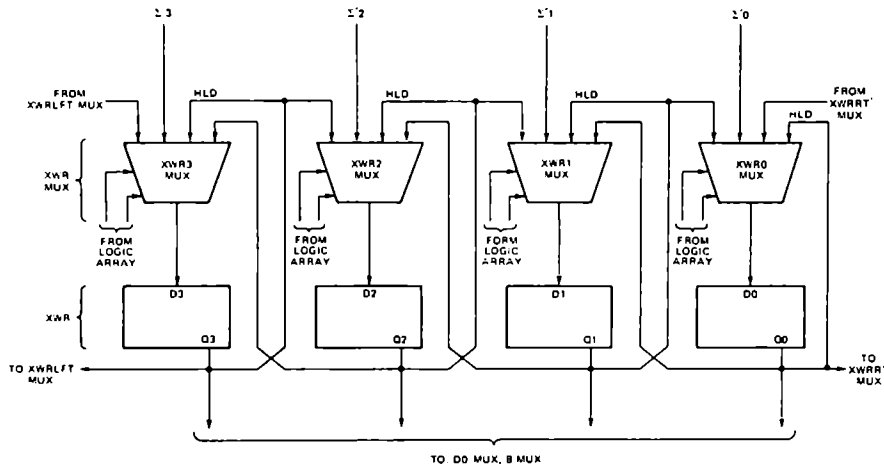


FIGURE 11 – EXTENDED WORKING REGISTER (XWR) AND XWR MULTIPLEXER

2.14 EXTENDED WORKING REGISTER MULTIPLEXER (XWR MUX)

The extended working register multiplexer provides source selection, including the bidirectional shifting capability, for the extended working register (see Figure 11). Under direction of the resident operation, the XWR MUX asynchronously selects either:

a. Σ' bus for ALU operand results
b. Hold mode for no change

c. Shift left
d. Shift right.

End conditions for both shift left and shift right operations are routed to or from XWR MSB (XWR3) or XWR LSB (XWR0) to the XWRLFT/XWRLFT' multiplexers or to the XWRRT/XWRRT' multiplexers respectively.

2.14.1 Σ-Bus, WR, XWR MSB Shift Transfer Multiplexers

The MSB shift transfers are accomplished by the WRLFT, XWRLFT input/output multiplexers and the WRLFT', XWRLFT' sum-bus/register MSB input multiplexers. All four multiplexers, and the impedance of the 3-state I/O lines of the WRLFT and XWRLFT multiplexer outputs are under control of the resident operation code and the relative position control (POS). Data paths of the multiplexers are illustrated in Figure 12, and bit transfers with respect to each of the shift operations are enumerated in Tables 11 through 14.

2.14.2 WRLFT, XWRLFT Multiplexers

The WRLFT, XWRLFT input/output multiplexers facilitate routing of the working register, extended working register, or sum bus MSB out the WRLFT, XWRLFT I/O's during output modes. In an input mode, the three-state output is at a high impedance permitting the WRLFT and/or the XWRLFT pins to be used as inputs.

2.14.3 WRLFT', XWRLFT' Multiplexers

The WRLFT' multiplexer selects the source for either the sum bus or working register MSB. Sign bit protection and right-shift bit-fill functions are all handled on-chip by these multiplexers under control of the operation code and relative position. The WRLFT' sources are:

a. WRLFT (input)
b. ALU carry out (for sign-fill)
c. Low level (for zero-fill)
d. XWRLFT input
e. XWR MSB
f. WR MSB (sign-fill in for RSA)
g. Sign fill in for RSA (see Figure 12)

The XWRLFT multiplexer selects the source for XWR MSB and provides sign-bit protection and right-shift-fill functions for the XWR. The XWRLFT sources are:

a. XWRLFT (input)
b. WRLFT
c. XWR MSB (sign-fill in for RSA)

2.14.4 WR, XWR LSB Shift Transfer Multiplexers

The LSB shift transfers are accomplished by the WRRT, XWRRT input/output multiplexers and the WRRT', XWRRT' sum-bus/register LSB input multiplexers. All four multiplexers, and the impedance of the 3-state I/O lines of the WRRT and XWRRT multiplexer outputs, are under control of the resident operation code and the relative position control (POS). Data paths of the multiplexers are illustrated in Figure 13.

2.14.5 WRRT Multiplexer, XWRRT Buffer

The WRRT input/output multiplexer facilitates routing of sum-bus or working register LSB out the WRRT I/O during output modes. The XWRRT I/O buffer can access and source the XWR LSB. In an input mode, the three-state output is at a high impedance permitting the WRRT and/or XWRRT pins to be used as inputs.

2.14.6 WRRT', XWRRT' Multiplexers

The WRRT' multiplexer selects either the WRRT input or a low logic level (fill) input as the LSB source for either the working register or the sum-bus. The XWRRT' multiplexer selects between the XWRRT input and low logic level (fill) input as the XWR LSB source.

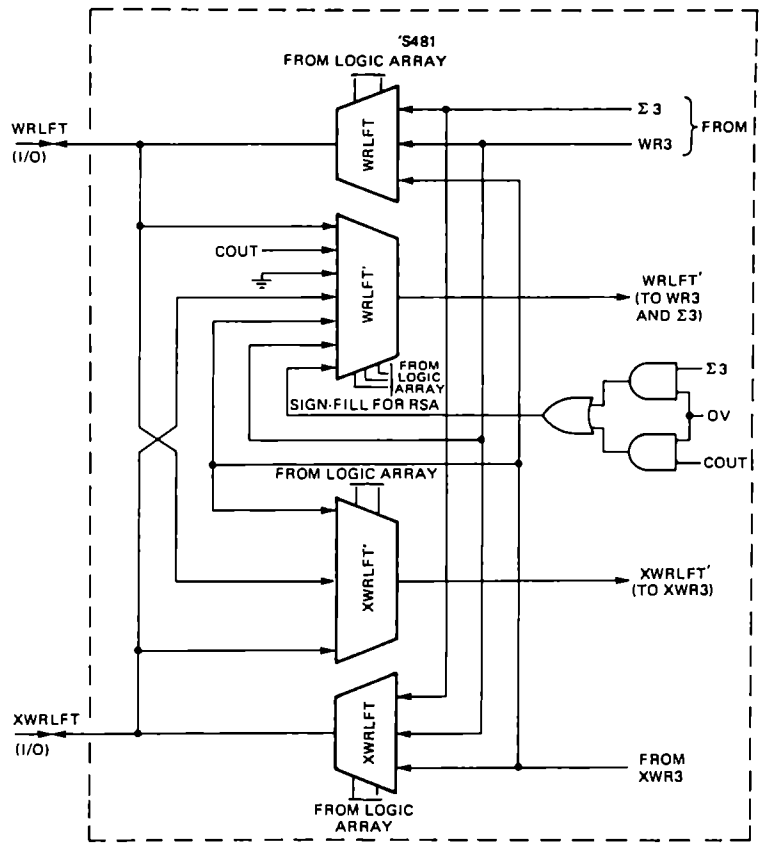


FIGURE 12 – SUM-BUS, WR, XWR MSB SHIFT TRANSFER MULTIPLEXERS

TABLE 11
WORKING REGISTER BIT TRANSFERS TO WRLFT/WRRT

SHIFT MODE	MOST-SIGNIFICANT POSITION				INTERMEDIATE POSITION				LEAST-SIGNIFICANT POSITION			
	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT
LSL (SP)	Z	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LSL (DP)	XWR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LSA (SP)	WR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	L	Z
LSA (DP)	XWR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LCIR (SP)	WR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
LCIR (DP)	XWR3	X	WRRT	Z	WR3	X	WRRT	Z	WR3	X	WRRT	Z
RSL (SP)	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	Z
RSL (DP)	Z	L	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RSA (SP)	Z	WR3	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RSA (DP)	Z	WR3	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RCIR (SP)	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0
RCIR (DP)	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0	Z	WRLFT	X	WR0

TABLE 12
SUM-BUS BIT TRANSFERS TO WRLFT/WRRT

SHIFT MODE	MOST-SIGNIFICANT POSITION				INTERMEDIATE POSITION				LEAST-SIGNIFICANT POSITION			
	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT	WRLFT	WRLFT'	WRRT'	WRRT
LSL (SP)	Z	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LSL (DP)	XWR3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LSA (SP)	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	L	Z
LSA (DP)	XWR3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LCIR (SP)	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
LCIR (DP)	XWR3	X	WRRT	Z	Σ3	X	WRRT	Z	Σ3	X	WRRT	Z
RSL (SP)	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RSL (DP)	Z	C-OUT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RSA (SP)	Z	*	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RSA (DP)	Z	*	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RCIR (SP)	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0
RCIR (DP)	Z	XWRLFT	X	Σ0	Z	WRLFT	X	Σ0	Z	WRLFT	X	Σ0

*VARIABLE = (Σ3 - ALU OVERFLOW) + (C-OUT - ALU OVERFLOW)

TABLE 13
EXTENDED WORKING REGISTER BIT TRANSFERS TO XWRLFT/XWRRT

SHIFT MODE	MOST-SIGNIFICANT POSITION				INTERMEDIATE POSITION				LEAST-SIGNIFICANT POSITION			
	XWRLFT	XWRLFT'	XWRRT'	XWRRT	XWRLFT	XWRLFT'	XWRRT'	XWRRT	XWRLFT	XWRLFT'	XWRRT'	XWRRT
LSL (SP)	Z	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
LSL (DP)	Z	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
LSA (SP)	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	L	Z
LSA (DP)	WR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	L	Z
LCIR (SP)	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
LCIR (DP)	WR3	X	XWRRT	Z	XWR3	X	XWRRT	Z	XWR3	X	XWRRT	Z
RSL (SP)	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	Z
RSL (DP)	Z	WRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RSA (SP)	Z	XWR3	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RSA (DP)	Z	WRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RCIR (SP)	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0
RCIR (DP)	Z	WRLFT	X	XWR0	Z	XWRLFT	X	XWR0	Z	XWRLFT	X	XWR0

TABLE 14
SUM-BUS BIT TRANSFERS TO XWRLFT (MSP)

SHIFT MODE	MOST-SIGNIFICANT POSITION XWRLFT	XWRLFT'	XWRRT'	XWRRT
LSL (SP)	Z	X	XWRRT	Z
LSL (DP)	Z	X	XWRRT	Z
LSA (SP)	XWR3	X	XWRRT	Z
LSA (DP)	Σ3	X	XWRRT	Z
LCIR (SP)	XWR3	X	XWRRT	Z
LCIR (DP)	Σ3	X	XWRRT	Z
RSL (SP)	Z	XWRLFT	X	XWR0
RSL (DP)	Z	WRLFT	X	XWR0
RSA (SP)	Z	XWR3	X	XWR0
RSA (DP)	Z	WRLFT	X	XWR0
RCIR (SP)	Z	XWRLFT	X	XWR0
RCIR (DP)	Z	WRLFT	X	XWR0

NOTE: Intermediate and Least-Significant Positions are the same as shown in Table 13.

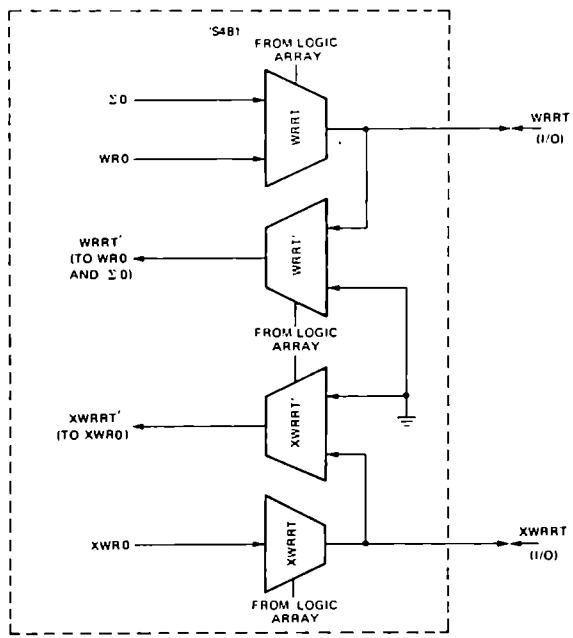


FIGURE 13 – SUM-BUS, WR, XWR LSB SHIFT TRANSFER MULTIPLEXERS

2.15 SHIFT FUNCTIONS

The 'S481 contains the necessary controls and data paths to perform single or double length logical, arithmetic, or circulate bidirectional shift functions in a single clock cycle. Each of the six shift functions implemented are selectable by a single microinstruction; and, additionally two single clock operation forms are included which provide the capability of performing an add/subtract in conjunction with a shift. The six shift functions and the basic operation forms offering them are enumerated in Table 15.

TABLE 15
MICROPROGRAMMABLE SHIFT FUNCTIONS

FUNCTION	OPERATION FORMS			
	SIMPLE SHIFT		ADD/SUBTRACT WITH SHIFT	
	SINGLE LENGTH	DOUBLE LENGTH	SINGLE LENGTH	DOUBLE LENGTH
LEFT CIRCULATE (LCIR)	IV, V	VI		
LEFT SHIFT ARITHMETIC (LSA)	IV, V	VI	III	
LEFT SHIFT LOGICAL (LSL)	IV, V	VI	III	II
RIGHT CIRCULATE (RCIR)	IV, V	VI		
RIGHT SHIFT ARITHMETIC (RSA)	IV, V	VI	III	
RIGHT SHIFT LOGICAL (RSL)	IV, V	VI	III	II

2.15.1 CIRCULATE (SHIFT) FUNCTIONS (MICROPROGRAMMABLE)

Operation forms IV and V provide the system designer with the capability of programming a single precision circulate (or rotate) of the Σ' bus, working register, or extended working register and operation form VI provides the capability of circulating or rotating a double-length word resident in the WR/XWR. A single-bit-position left or right circulate is accomplished on each clock without the loss of any bits as the shift transfer multiplexers, under control of the resident operation and position input, interconnect the bus or register as illustrated in Figure 14.

The remaining end conditions are handled on chip by the shift transfer multiplexers to interconnect the bit transfer mechanisms for MSB ↔ LSB for single precision circulates and for transfers to or from the Σ' bus or working register and the extended working register during double-precision circulates. Data flow between packages in an expanded word-length system is via the interconnected WRRT/WRLFT and XWRRT/XWRLFT terminals.

2.15.2 ARITHMETIC SHIFT FUNCTIONS (MICROPROGRAMMABLE)

Operation forms III, IV, V and VI provide the system designer with the capability of programming the following arithmetic shifts.

Form III – A single-precision arithmetic left or sign-protected right shift of the sum or difference of the A and B operands destined for either the WR or XWR.

Form IV – A single-precision arithmetic left or sign-protected right shift of the A operand destined for the Σ' bus.

Form V – A single-precision arithmetic left or sign-protected right shift of the WR or XWR contents.

Form VI – A double-precision arithmetic left or sign-protected right shift of the WR and XWR contents.

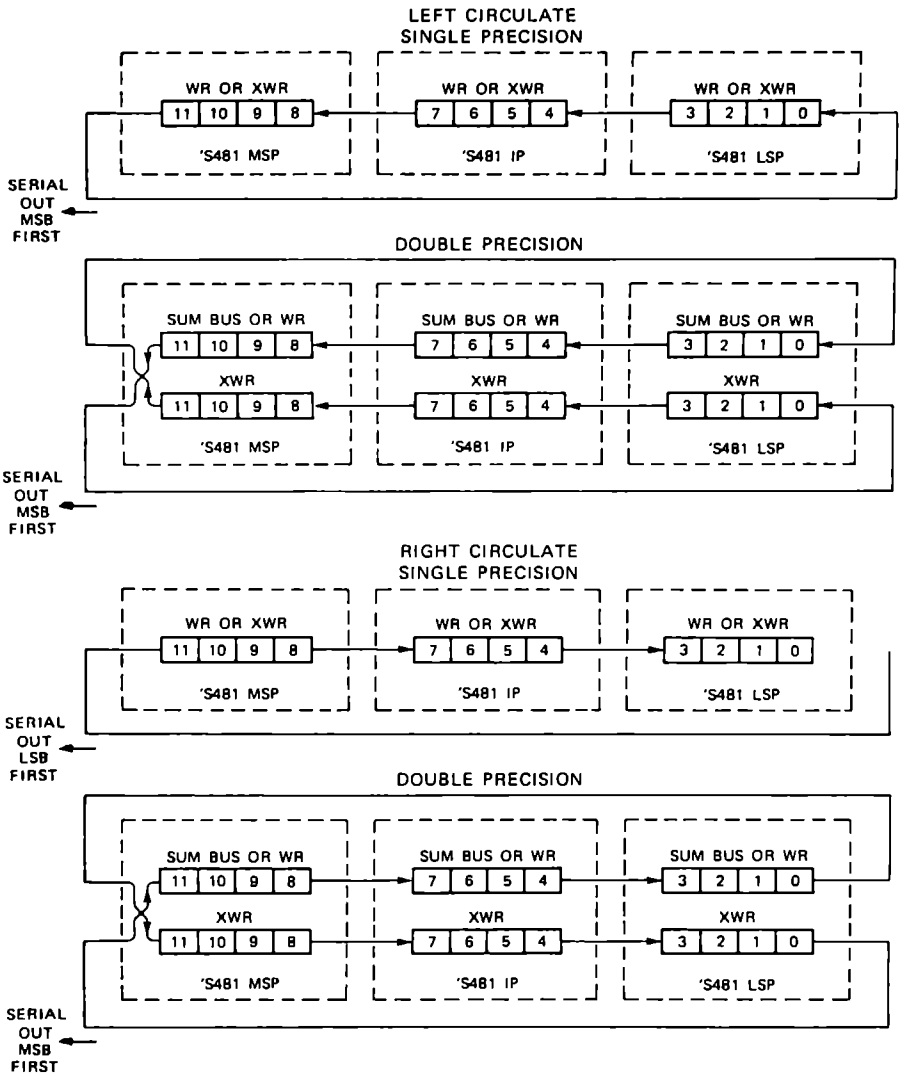


FIGURE 14 – CIRCULATE FUNCTIONS

A single-bit-position shift is accomplished on each clock with right-shift sign-protection and left shift LSB zero-fill operations controlled by the shift transfer multiplexers under direction of the resident operation and the position input. See Figure 15.

The remaining end conditions are handled on chip by the shift transfer multiplexers to interconnect the bit transfer mechanisms for transfers to or from the Σ' bus or working register and the extended working register during double-precision arithmetic shifts. Data flow between packages in an expanded word-length system is via the interconnected WRRT/WRLFT and XWRRT/XWRLFT terminals.

2.15.3 LOGICAL SHIFT FUNCTIONS (MICROPROGRAMMABLE)

Operation Forms II, III, IV, V and VI provide the system designer with the capability of programming the following logical shifts:

Form II – A double-precision left or right shift of the sum or difference of the A and B operands destined for the WR in conjunction with the XWR.

Form III – A single-precision left or right logical shift of the sum or difference of the A and B operands destined for the WR or the XWR.

Form IV – A single-precision left or right logical shift of the A operand destined for the Σ' bus.

Form V – A single-precision left or right logical shift of the WR or XWR contents.

Form VI – A double-precision left or right logical shift of the WR and XWR contents.

A single-bit-position shift is accomplished on each clock with MSB and LSB fill operations controlled by the shift transfer multiplexers under direction of the resident operation and the position input. See Figure 16.

The remaining end conditions are handled on chip by the shift transfer multiplexers to interconnect the bit transfer mechanisms for transfers to and from the Σ' bus or working register and the extended working register during double-precision logical shifts. Data flow between packages in an expanded word length system is via the interconnected WRRT/WRLFT and XWRRT/XWRLFT terminals.

2.16 DATA-OUT PORT MULTIPLEXER (DO MUX)

The data-out port multiplexer, Figure 17, provides selection for routing the contents of either the sum'-bus, working register, or extended working register to the parallel output port. Additionally, the multiplexer is equipped with 3-state outputs providing the capability to isolate the 'S481 from the system data bus. Source selections and high-impedance controls are detailed in Table 16.

Each data output is capable of sourcing 6.5 and sinking 10 milliamperes of drive current.

2.17 MEMORY AND PROGRAM COUNTERS

Dual counters provide the system designer with a processor element containing both an iteration counter and the capability of generating and/or storing locations of operands/data.

Either counter can be loaded or preset to any value or result from the sum bus in operations forms as follows:

	SELECTABLE AS DESTINATION	
OP FORM	PC	MC
I	Yes	Yes
III	No	Yes
VIII	Yes	No

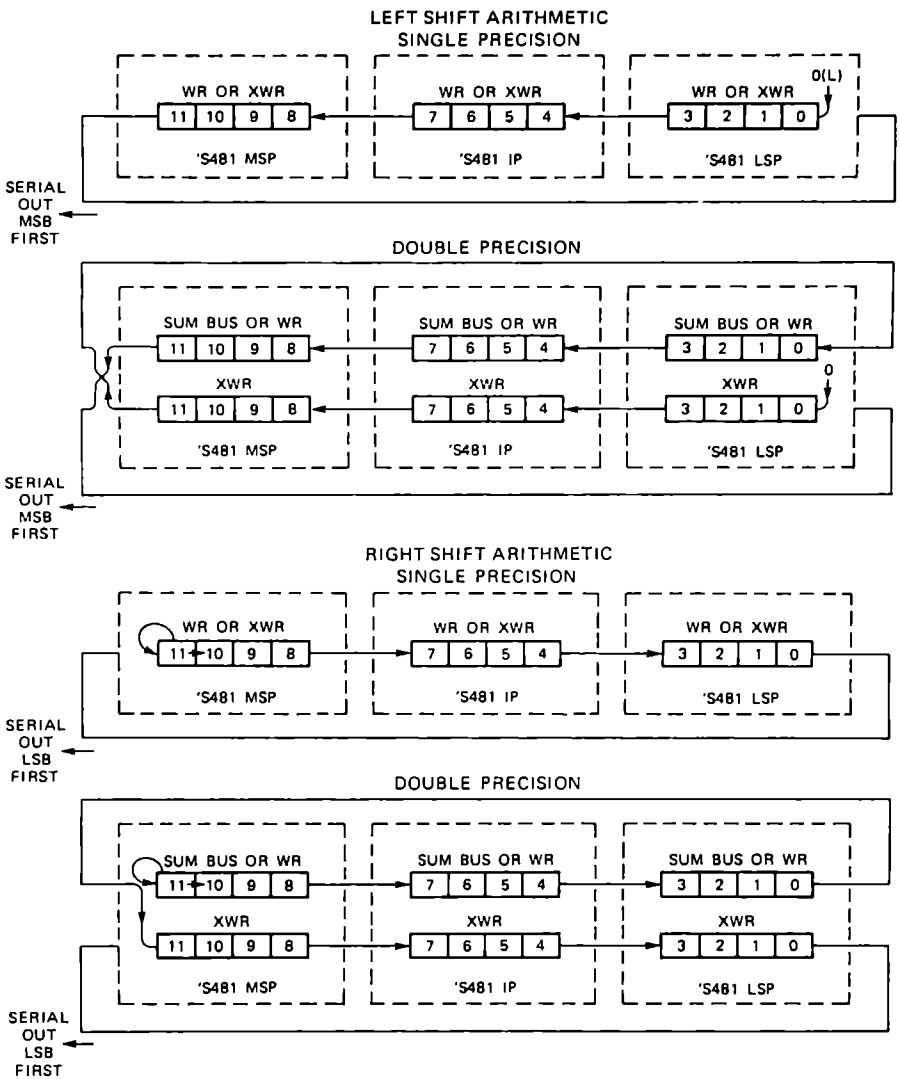


FIGURE 15 – ARITHMETIC SHIFT FUNCTIONS

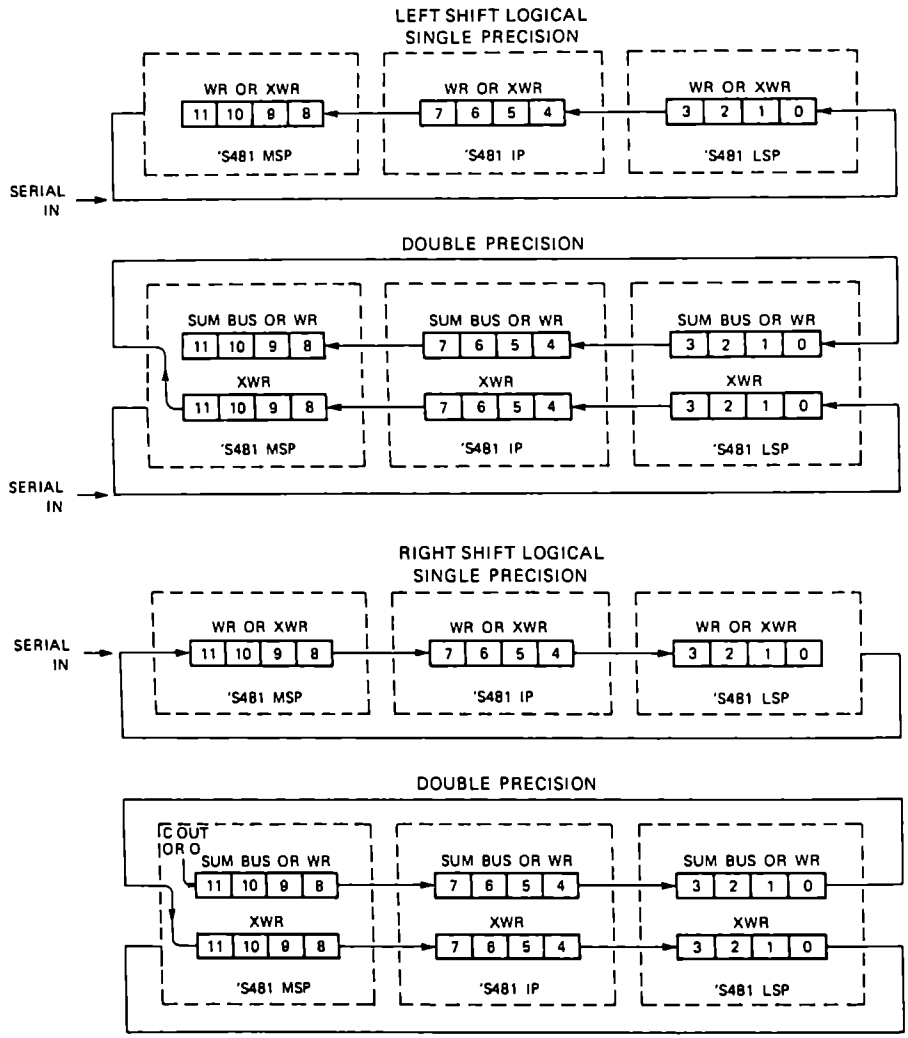


FIGURE 18 – LOGICAL SHIFT FUNCTIONS

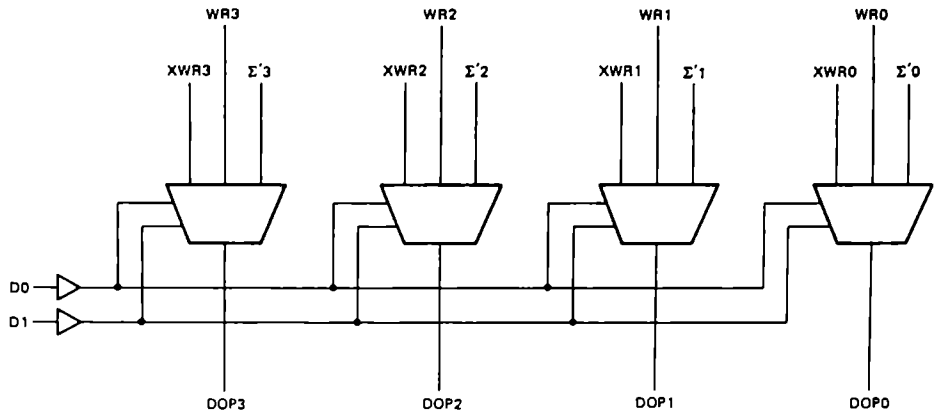


FIGURE 17 – DATA-OUT PORT MULTIPLEXER (DO MUX)

Under control of the position (POS) input and the resident operation code, the $\overline{CCO}$/OV output facilitates cascading the program and memory counters. In the least-significant and intermediate positions, the $\overline{CCO}$ pins of lesser significant packages are connected to the $\overline{CCI}$ pins of more significant packages to complete the counter interconnections to the bit-size of the processor element.

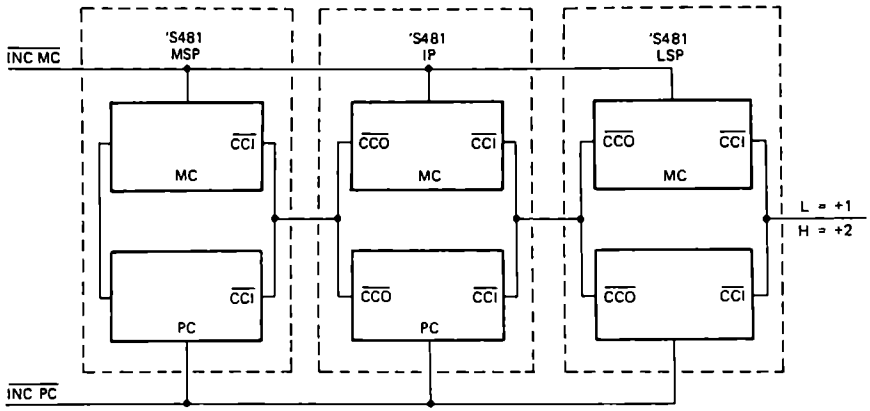
TABLE 16
DATA-OUT PORT CONTROL

CONTROL INPUTS		SOURCE OR FUNCTION
D1	D0	
L	L	Σ'-BUS
L	H	EXTENDED WORKING REGISTER
H	L	WORKING REGISTER
H	H	HIGH-IMPEDANCE

The functionally identical program and memory counters, sharing a common counter carry input ($\overline{CCI}$) control pin and a common counter carry output ($\overline{CCO}$) pin, feature individual control lines ($\overline{INC\ PC}$, $\overline{INC\ MC}$) which can be used to instruct either (but normally not both) or neither counter to increment on the next clock transition in any of the 14 operation forms. Additionally, the counter in the LSP, under command of the POS input, has the capability of incrementing its value by one or by two to facilitate the generation of even or odd address locations in a single clock cycle. Contents of the counters can be read out from the address out port asynchronously under control of the address output multiplexer (AO MUX) select input.

Typical counter functions with respect to package relative positions are shown in Figure 18.

In the MSP, the $\overline{CCO}$/OV output, as a result of the position (POS) control, becomes the ALU/shift overflow (OV) status output.



INPUTS			CK	COUNTER VALUE			
INC PC	INC MC	CCI		LSP MC	LSP PC	MSP, IP MC	MSP, IP PC
H	H	X	↑	NO CHG	NO CHG	NO CHG	NO CHG
L	H	L	↑	NO CHG	+1	NO CHG	+1
L	H	H	↑	NO CHG	+2	NO CHG	NO CHG
H	L	L	↑	+1	NO CHG	+1	NO CHG
H	L	H	↑	+2	NO CHG	NO CHG	NO CHG
X	X	X	L	NO CHG	NO CHG	NO CHG	NO CHG
X	X	X	H	NO CHG	NO CHG	NO CHG	NO CHG

H=HIGH LEVEL, L=LOW LEVEL, X=IRRELEVANT, ↑=LOW-TO-HIGH TRANSITION

FIGURE 18 – PROGRAM AND MEMORY COUNTER FUNCTIONS

2.18 ADDRESS-OUT PORT MULTIPLEXER (AO MUX)

The address-out port multiplexer, Figure 19, provides for direct parallel access to the contents of either the program or memory counter contents. A single line controls selection as shown in Table 17.

TABLE 17
ADDRESS-OUT PORT CONTROL

CONTROL INPUT A0	COUNTER SELECTED
L	MEMORY
H	PROGRAM

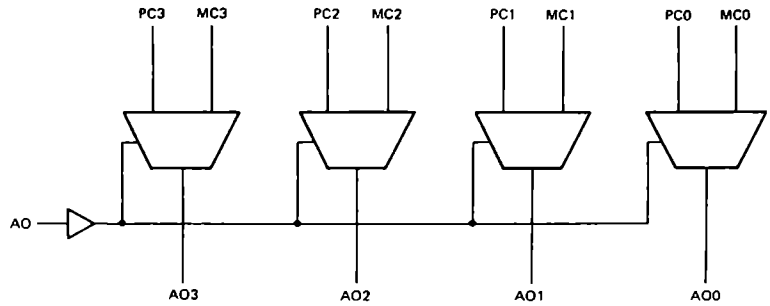


FIGURE 19 – ADDRESS-OUT PORT MULTIPLEXER (AO MUX)

2.19 EXPANDING THE WORD LENGTH

The 'S481 processor element contains on-chip personality circuitry designed specifically to minimize the external discrete components required to cascade 4-bit slices to form larger word lengths. At the processor-element level, three external resistors are all that is required: one to pull-up the open-collector outputs and two to establish the position control input voltage at the LSP. Figure 20 shows a typical 16-bit processor element and illustrates the parallel bus arrangements for I/O and control with an SN74S182 performing ALU look-ahead across the 16-bit word. Interconnectivity for the shift, arithmetic, and counter functions is accomplished by hardwiring the functions as shown.

At the system level, standard techniques commonly employed for power-supply bypass, termination of unused pins, and system grounding of high-performance Schottky TTL systems are recommended.

3. OPERATIONAL DESCRIPTIONS

3.1 MICRO/MACRO-OPERATIONS

The micro/macro-operations resident in the micro-decode logic array can be accessed with an eleven-bit operation-select word. Operational flexibility is maximized by the fact that the op-select word format has been defined individually for each of the 14 different operation forms.

Operation Forms I, II, and III are primarily ALU functions. Forms II and III combine logical or arithmetic shifting functions with the ALU result. Form II can be used for double-precision shifting. Sources, specific ALU function, shift format, and destinations are detailed for each op-select word format.

Forms IV, V, and VI perform either logical or arithmetic, bidirectional shifting of the single- and double-precision buses and registers.

Form VII can be used to compare the magnitude of A source to B source, or B source to A source.

Form VIII provides the capability to logically combine the values of the A and B sources.

Form IX zeros the Σ' bus with the effect of providing no operation.

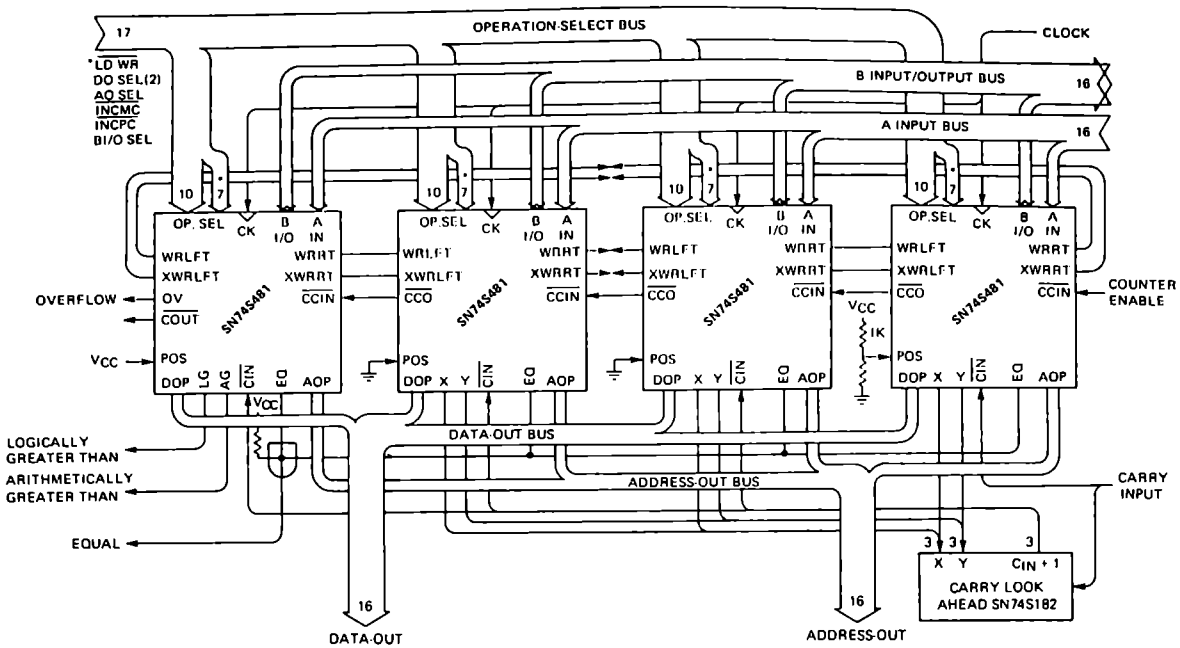


FIGURE 20 – TYPICAL 16-BIT PROCESSOR

Forms X through XIV are macroprogrammable operations which provide:

a. CRC partial sum update (normally $\frac{N}{2}$ clocks)
b. Signed Divide (N + 3 clocks)
c. Unsigned Divide (N + 1 clocks)
d. N-bit-by-N-bit double-precision unsigned multiply (N clocks)
e. N-bit-by-N-bit double-precision signed multiply (N clocks)

The 14 operation forms, symbols, and number of unique operations are detailed in Table 18.

TABLE 18
OPERATION FORM SUMMARY

FORM	MICRO/MACRO – OPERATION FORMS	NO. OF OPS
I	A PLUS B PLUS ALUCIN ⟶ Σ' BUS ONLY	4,096
	A PLUS B PLUS ALUCIN ⟶ WR, XWR, PC, OR MC	8,192
II	B PLUS A PLUS ALUCIN DOUBLE-PRECISION SHIFTED ⟶ WR and XWR	384
III	A PLUS B PLUS ALUCIN SHIFTED ⟶ WR OR XWR	1,536
IV	A SHIFTED ⟶ Σ' BUS	192
V	WR SHIFTED ⟶ WR	192
	XWR SHIFTED ⟶ XWR	192
VI	WR AND XWR DOUBLE-PRECISION SHIFTED ⟶ WR AND XWR	256
VII	A : B OR B : A (COMPARE)	512
VIII	A NOR B ⟶ WR, XWR, PC OR B IN/OUT	3,072
	A OR B ⟶ WR, XWR, PC OR B IN/OUT	3,072
	A EX-OR B ⟶ WR, XWR, PC OR B IN/OUT	3,072
IX	ZERO ⟶ Σ' BUS (NO OP)	1
X	CRC CALCULATION (N CLK TIMES, CRC PARTIAL SUM IN WR)	1
XI	N-BIT QUOTIENT (WITH R) SIGNED DIVIDE (N+3 CLK TIMES)	5
XII	N-BIT QUOTIENT (WITH R) UNSIGNED DIVIDE (N+1 CLK TIMES)	3
XIII	N-BIT BY N-BIT DOUBLE-PRECISION UNSIGNED MULTIPLY (N CLK TIMES)	1
XIV	N-BIT BY N-BIT DOUBLE-PRECISION SIGNED MULTIPLY (N CLK TIMES)	1
	TOTAL OPERATIONS	24,780

3.2 OPERATION FORM I – ADD/SUBTRACT → REGISTER

Operation Form I is designed specifically to perform the addition or symmetrial subtraction of two operands. The operation form shown in Figure 21, is composed of two distinct capabilities:

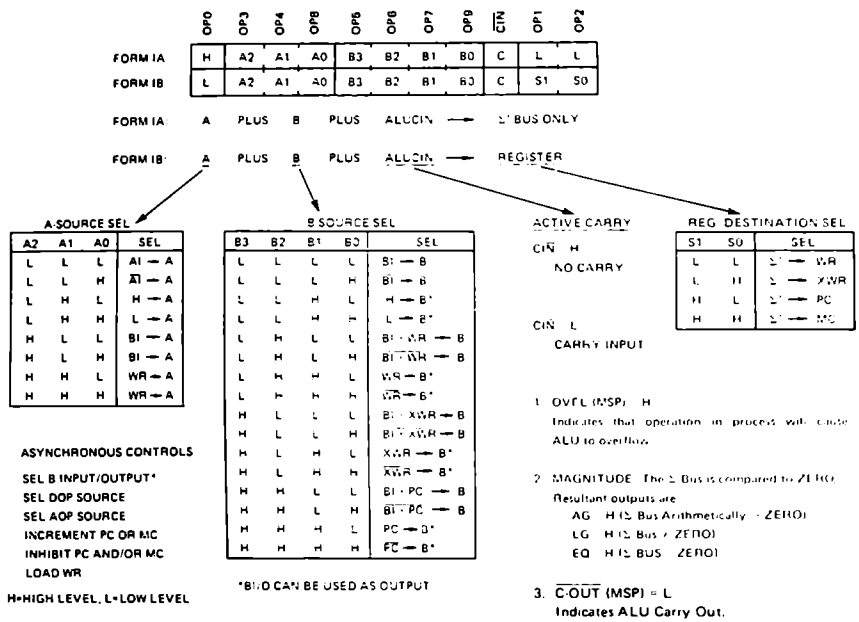

OP0 OP3 OP4 OP8 OP5 OP6 OP7 OP9 CIN OP1 OP2
FORM IA H A2 A1 A0 B3 B2 B1 B0 C L L
FORM IB L A2 A1 A0 B3 B2 B1 B0 C S1 S0
FORM IA A PLUS B PLUS ALUCIN → Σ' BUS ONLY
FORM IB A PLUS B PLUS ALUCIN → REGISTER
A SOURCE SEL
A2 A1 A0 SEL
L L L A1 → A
L L H A1 → A
L H L H → A
L H H L → A
H L L B1 → A
H L H B1 → A
H H L WR → A
H H H WR → A
B SOURCE SEL
B3 B2 B1 B0 SEL
L L L L B1 → B
L L L H B1 → B
L L H L H → B*
L L H H L → B*
L H L L B1 ⊕ WR → B
L H L H B1 ⊕ WR → B
L H H L WR → B*
L H H H WR → B*
H L L L B1 ⊕ WR → B
H L L H B1 ⊕ WR → B
H L H L X⊕R → B*
H L H H X⊕R → B*
H H L L B1 ⊕ PC → B
H H L H B1 ⊕ PC → B
H H H L PC → B*
H H H H PC → B*
ACTIVE CARRY
CIN H
NO CARRY
CIN L
CARRY INPUT
REG DESTINATION SEL
S1 S0 SEL
L L Σ' → WR
L H Σ → X⊕R
H L Σ' → PC
H H Σ' → MC
1 OVFL (MSP) H
Indicates that operation in process will cause ALU to overflow
2 MAGNITUDE The Σ Bus is compared to ZERO
Resultant outputs are
AG H (Σ Bus Arithmetically > ZERO)
LG H (Σ Bus < ZERO)
EQ H (Σ BUS = ZERO)
3. C-OUT (MSP) = L
Indicates ALU Carry Out.
ASYNCHRONOUS CONTROLS
SEL B INPUT/OUTPUT*
SEL DOP SOURCE
SEL AOP SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR
H=HIGH LEVEL, L=LOW LEVEL
*B1:0 CAN BE USED AS OUTPUT

FIGURE 21 – FORM I–ARITHMETIC OPERATIONS: A PLUS B PLUS ALUCIN → { Σ' BUS / REGISTER }

a. Form IA provides the capability of adding or subtracting two operands and routing the results to the Σ' bus. Symbolically, this operation can be expressed as:

$$A \begin{Bmatrix} \text{PLUS} \\ \text{MINUS} \end{Bmatrix} B \text{ PLUS ALUCIN} \rightarrow \Sigma' \text{ BUS}$$

This form provides the capability of choosing from any one of the A and any one of the B sources listed in Figure 21 as the operands to accomplish the add/subtract. The example illustrated in Figure 22 utilizes the I/O capability of the B input/output port. Input data at the AI or B I/O is setup and then latched into the 'S481 A or B input latch on the negative transition of the 'S481 clock.

During Form IA operations, the contents of the extended working register are not changed and the working register may be saved or loaded directly. The program or memory counters under control of the asynchronous increment, inhibit, and LSP $\overline{CCI}$ can be saved or either may be incremented by one or two. Sources for the DOP and AOP are also selectable.

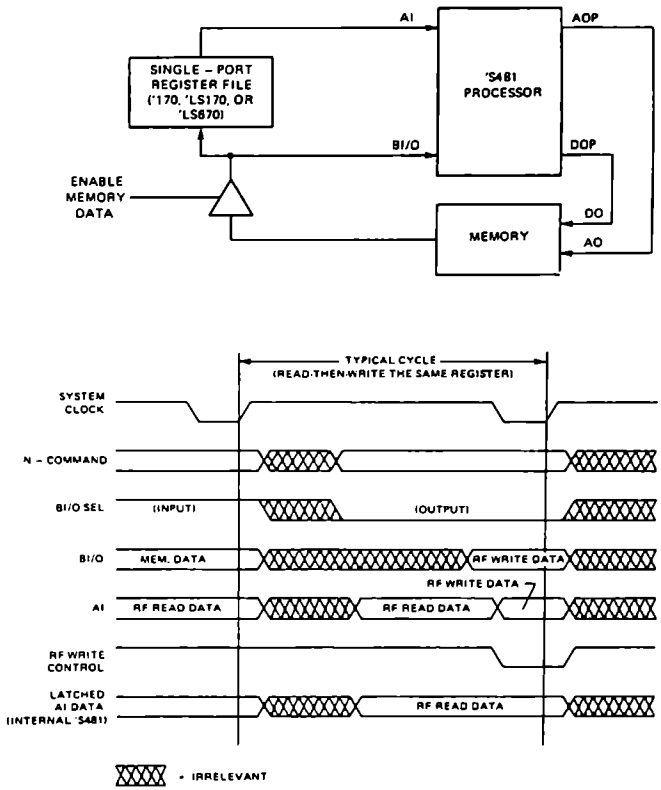


FIGURE 22 – 'S481 OPERATION WITH SINGLE-PORT REGISTER FILE

The overflow and magnitude status lines are active as enumerated in Figure 21.

b. Form 1B provides the capability of adding or subtracting two operands and routing the results to one of the four 'S481 storage destinations: the working register (WR), the extended working register (XWR), the program counter (PC), or the memory counter (MC). Symbolically, this operation can be expressed as:

$$A \left| \begin{matrix} \text{PLUS} \\ \text{MINUS} \end{matrix} \right| \text{B PLUS ALUCIN} \rightarrow \text{REGISTER}$$

This form provides the capability of choosing from any one of the A and any one of the B sources listed in Figure 21 as the operands to accomplish the add/subtract.

3.3 OPERATION FORM II – ADD/SUBTRACT WITH DOUBLE-PRECISION SHIFT

Operation Form II is designed specifically to perform one of two classical iterations used frequently to implement microprogrammed multiply and divide algorithms. This form provides the system designer with the capability of selecting a single microinstruction which will complete both the add-and-shift or subtract-and-shift functions in a single clock cycle. Available microinstructions are illustrated in Figure 23. Symbolically, Form II operations can be represented as:

(A PLUS B PLUS ALUCIN)	SHIFTED → WR, XWR
(B MINUS A MINUS 1)	SHIFTED → WR, XWR

Hardwired algorithms for double-precision multiply and divide routines can be selected in operation forms XI, XII, XIII, or XIV.

During Form II operations the status, overflow, and asynchronous controls are the same as described for Form I.

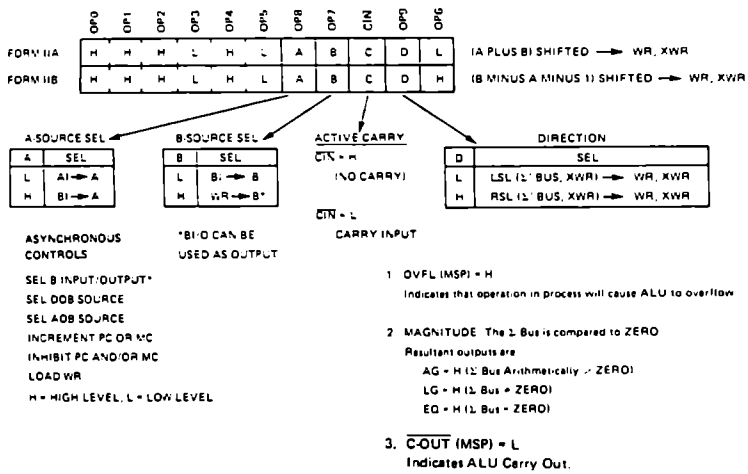

OP0 OP1 OP2 OP3 OP4 OP5 OP8 OP7 CIN OP9 OP6
FORM IIA H H H L H L A B C D L
(A PLUS B) SHIFTED → WR, XWR
FORM IIB H H H L H L A B C D H
(B MINUS A MINUS 1) SHIFTED → WR, XWR
A-SOURCE SEL
A SEL
L A|-→A
H B|-→A
B-SOURCE SEL
B SEL
L B|-→B
H WR-→B*
ACTIVE CARRY
CIN = H
(NO CARRY)
CIN = L
CARRY INPUT
DIRECTION
D SEL
L LSL (Σ BUS, XWR) → WR, XWR
H RSL (Σ BUS, XWR) → WR, XWR
ASYNCHRONOUS CONTROLS
SEL B INPUT/OUTPUT*
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR
H = HIGH LEVEL, L = LOW LEVEL
*B I/O CAN BE USED AS OUTPUT
1 OVFL (MSP) = H
Indicates that operation in process will cause ALU to overflow
2 MAGNITUDE The Σ Bus is compared to ZERO
Resultant outputs are
AG = H (Σ Bus Arithmetically > ZERO)
LG = H (Σ Bus ≠ ZERO)
EQ = H (Σ Bus = ZERO)
3. C-OUT (MSP) = L
Indicates ALU Carry Out.

FIGURE 23 – FORM II–ARITHMETIC WITH DOUBLE-PRECISION SHIFT

$$\begin{vmatrix} A \\ B \end{vmatrix} \text{ PLUS } \begin{vmatrix} B \\ A \end{vmatrix} \text{ PLUS CARRY SHIFTED} \rightarrow \text{WR, XWR}$$

(MULTIPLY AND DIVIDE SHIFT OPERATIONS WITHOUT AUTOMATIC CONTROL)

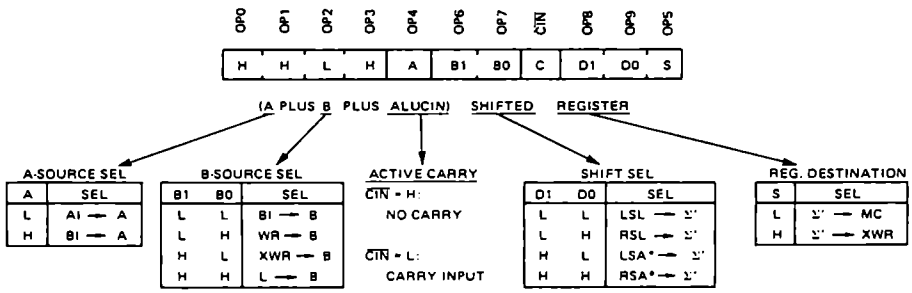
3.4 OPERATION FORM III – ADD WITH SINGLE-PRECISION SHIFT

Operation Form III is a universal microinstruction providing the designers with the capability of performing an add-and-shift function in a single clock cycle. Sources and destinations are shown in Figure 24. Also enumerated are the shift functions which are selectable as part of the microinstruction.

Magnitude and overflow status indicators are active as enumerated in Figure 24. Form III can be represented symbolically as:

(A PLUS B PLUS ALUCIN) SHIFTED → XWR, OR MC

During Form III operation the contents of the working register are not changed unless an asynchronous load is selected. If not selected as the destination, the extended working register will be saved. The memory counter can be the operand destination, or it and the program counter can be saved, or one can be incremented by one or two on selection. Sources for the DOP and AOP are also selectable.


OP0 OP1 OP2 OP3 OP4 OP6 OP7 C̄IN OP8 OP9 OP5
H H L H A B1 B0 C D1 D0 S
(A PLUS B PLUS ALUCIN) SHIFTED REGISTER
A-SOURCE SEL
A SEL
L AI → A
H BI → A
B-SOURCE SEL
B1 B0 SEL
L L BI → B
L H WR → B
H L XWR → B
H H L → B
ACTIVE CARRY
C̄IN = H:
NO CARRY
C̄IN = L:
CARRY INPUT
SHIFT SEL
D1 D0 SEL
L L LSL → Σ'
L H RSL → Σ'
H L LSA* → Σ'
H H RSA* → Σ'
REG. DESTINATION
S SEL
L Σ' → MC
H Σ' → XWR

ASYNCHRONOUS CONTROLS:

- SEL B INPUT/OUTPUT
- SEL DOB SOURCE
- SEL AOB SOURCE
- INCREMENT PC OR MC
- INHIBIT PC AND/OR MC
- LOAD WR

H = HIGH LEVEL, L = LOW LEVEL

1. OVFL (MSP) = H Indicates that the shift operation in process will cause the selected register to overflow.
2. *MAGNITUDE. During LSA or RSA, A plus C (N1) is compared to $\overline{B}$ (N2); during the remaining operations, the Σ Bus is compared to ZERO. Resultant outputs are:
   AG = H (N1 ARITHMETICALLY > N2) or (Σ BUS ARITHMETICALLY > ZERO)
   LG = H (N1 > N2) or (Σ BUS ≠ ZERO)
   EQ = H (N1 = N2) or (Σ BUS = ZERO)
3. $\overline{COUT}$ (MSP) = L Indicates ALU Carry Out.

FIGURE 24 – FORM III–ARITHMETIC WITH SINGLE-PRECISION SHIFT
(A PLUS B PLUS ALUCIN) SHIFTED → XWR OR MC

3.5 OPERATION FORM IV – AI SHIFTED → Σ' BUS

Operation Form IV is designed specifically for performing a single bit-position logical, arithmetic, or circular shift of the data applied at the A input port. This single clock operation can be used to shift information residing in any of the external working memory register locations simply by enabling the output capability of the BI/O port and writing the shifted word back into the same (or any other selected) memory location.

Asynchronous controls are the same as described for Operation Form IA, and the magnitude status lines are active and overflow is active during left-shift arithmetic (LSA) operation as enumerated in Figure 25.

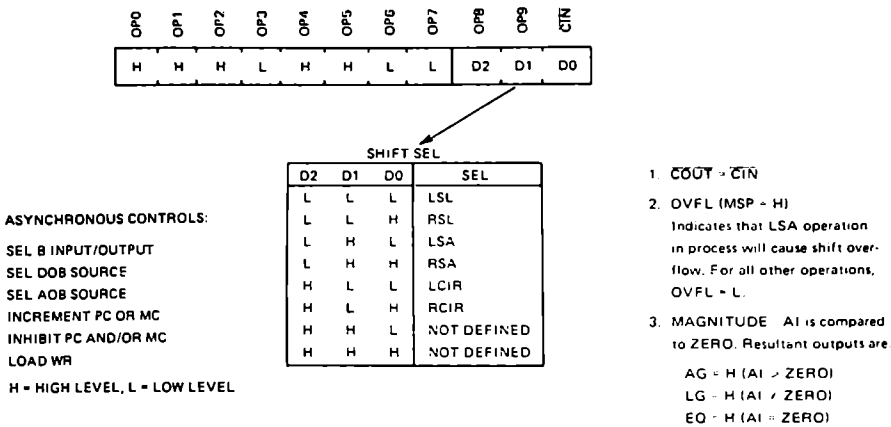

OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7 OP8 OP9 CIN
H H H L H H L L D2 D1 D0
SHIFT SEL
D2 D1 D0 SEL
L L L LSL
L L H RSL
L H L LSA
L H H RSA
H L L LCIR
H L H RCIR
H H L NOT DEFINED
H H H NOT DEFINED
ASYNCHRONOUS CONTROLS:
SEL B INPUT/OUTPUT
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR
H = HIGH LEVEL, L = LOW LEVEL
1. COUT = CIN
2. OVFL (MSP = H)
Indicates that LSA operation in process will cause shift overflow. For all other operations, OVFL = L.
3. MAGNITUDE AI is compared to ZERO. Resultant outputs are
AG = H (AI > ZERO)
LG = H (AI < ZERO)
EQ = H (AI = ZERO)

FIGURE 25 – FORM IV–AI SHIFTED → Σ BUS

3.6 OPERATION FORM V – SINGLE-LENGTH SHIFT

Operation Form V performs a single-bit position, logical, arithmetic, or circular shift of either the working register or extended working register. Magnitude status indicators are active and overflow is active during left-shift arithmetic (LSA) operations as enumerated in Figure 26. Asynchronous controls are the same as described for Operation Form IA.

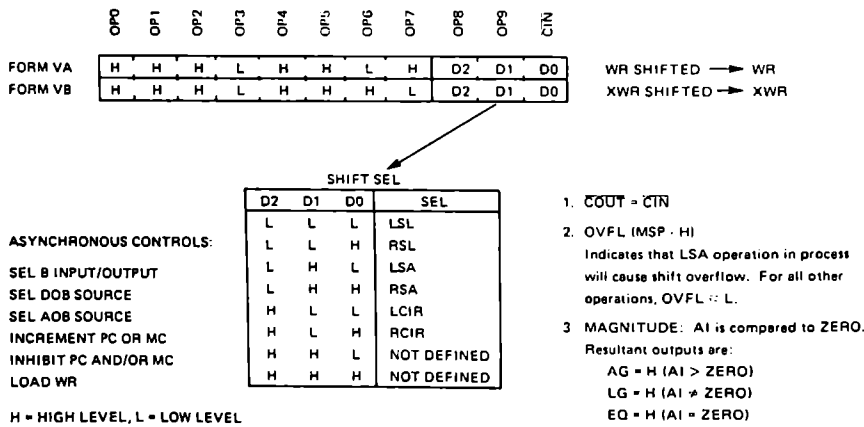

OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7 OP8 OP9 CIN
FORM VA H H H L H H L H D2 D1 D0
FORM VB H H H L H H H L D2 D1 D0
WR SHIFTED → WR
XWR SHIFTED → XWR
SHIFT SEL
D2 D1 D0 SEL
L L L LSL
L L H RSL
L H L LSA
L H H RSA
H L L LCIR
H L H RCIR
H H L NOT DEFINED
H H H NOT DEFINED
ASYNCHRONOUS CONTROLS:
SEL B INPUT/OUTPUT
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR
H = HIGH LEVEL, L = LOW LEVEL
1. COUT = CIN
2. OVFL (MSP = H)
Indicates that LSA operation in process will cause shift overflow. For all other operations, OVFL = L.
3 MAGNITUDE: AI is compared to ZERO. Resultant outputs are:
AG = H (AI > ZERO)
LG = H (AI ≠ ZERO)
EQ = H (AI = ZERO)

FIGURE 26 – FORM V: $\left\{\begin{matrix}\text{WR}\\\text{XWR}\end{matrix}\right\}$ SHIFTED → $\left\{\begin{matrix}\text{WR}\\\text{XWR}\end{matrix}\right\}$

3.7 OPERATION FORM VI – DOUBLE-PRECISION SHIFTS

Operation Form VI performs a double-precision logical, arithmetic, or circular shift of a double-length word residing in the working register and extended working register. Magnitude status indicators are active and overflow is active during left-shift arithmetic (LSA) operations as enumerated in Figure 27. Asynchronous controls are the same as described for operation form IA.

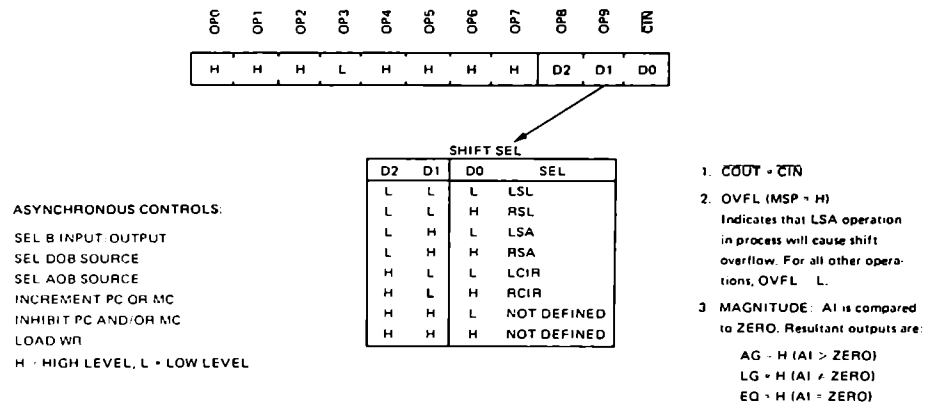

OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7 OP8 OP9 CIN
H H H L H H H H D2 D1 D0
SHIFT SEL
D2 D1 D0 SEL
L L L LSL
L L H RSL
L H L LSA
L H H RSA
H L L LCIR
H L H RCIR
H H L NOT DEFINED
H H H NOT DEFINED
ASYNCHRONOUS CONTROLS:
SEL B INPUT/OUTPUT
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR
H = HIGH LEVEL, L = LOW LEVEL
1. COUT = CIN
2. OVFL (MSP = H)
Indicates that LSA operation in process will cause shift overflow. For all other operations, OVFL = L.
3 MAGNITUDE: AI is compared to ZERO. Resultant outputs are:
AG = H (AI > ZERO)
LG = H (AI ≠ ZERO)
EQ = H (AI = ZERO)

FIGURE 27 – FORM VI–DOUBLE-PRECISION SHIFTS: (WR, XWR)SHIFTED →(WR, XWR)

3.8 OPERATION FORM VII – COMPARE (A:B OR B:A)

Operation Form VII is designed specifically to provide the system designer with the capability of symmetrically comparing either operands A-to-B or operands B-to-A. The operands selectable are enumerated in Figure 28 as the A source select or B source select. The carry output, overflow, and magnitude status lines decode and indicate the logical and arithmetic relationship of the operands being compared as shown in Figure 28. Asynchronous controls are the same as described for Operation Form IA.

3.9 OPERATION FORM VIII – LOGICAL FUNCTIONS

The ALU with its carry circuit functionally inactivated in Form VIII operations can be microprogrammed in conjunction with the source operands to perform any of the possible combinatorial Boolean functions on two binary variables. See Figure 29. Simple transfer functions are performed with the arithmetic operations in Form I, and combinatorial transfer and shift operations are available in Form III.

As with the arithmetic operations, a highly flexible source selection extends performance of single clock combinatorial logical operations between two (external) operands applied at the A and B input ports, or combinations of resident data in 'S481 registers or counters can be combined logically with another register or external source. The specific combinations selectable are enumerated in the following paragraphs.

	OP0	OP1	OP2	OP3	OP4	OP8	OP5	OP6	OP7	OP9	CIN	N1:N2
FORM VIIA	H	H	H	L	L	A	B2	B1	B0	L	H	A : B
FORM VIIB	H	H	H	L	L	A	B2	B1	B0	H	H	B : A

A-SOURCE SEL

A	SEL
L	AI
H	WR

B-SOURCE SEL

B2	B1	B0	SEL
L	L	L	BI
L	L	H	H*
L	H	L	BI · WR
L	H	H	WR*
H	L	L	BI · XWR
H	L	H	XWR*
H	H	L	BI · PC
H	H	H	PC*

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT*
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR

*BI/O CAN BE USED AS OUTPUT (Σ BUS = N1–N2–1)

1. $\overline{COUT}$ = LG
2. MAGNITUDE: A or B (N1) is compared to B or A (N2), respectively. The resultant outputs are:
   - AG = H (N1 arithmetically > N2)
   - LG = H (N1 logically > N2)
   - EQ = H (N1 = N2)
3. OVFL (MSP) IS NOT DEFINED.

H = HIGH LEVEL, L = LOW LEVEL

FIGURE 28 – FORM VII–COMPARE: $\begin{vmatrix} A : B \\ B : A \end{vmatrix}$

	OP0	OP1	OP2	OP3	OP4	OP8	OP6	OP7	OP9	OP5	CIN	
FORM VIIA	H	L	H	L	A1	A0	B2	B1	B0	S1	S0	NOR
FORM VIIB	H	L	H	H	A1	A0	B2	B1	B0	S1	S0	OR
FORM VIIC	H	H	L	L	A1	A0	B2	B1	B0	S1	S0	EX-OR

A { NOR / OR / X-OR } B → REG

A-SOURCE SEL

A1	A0	SEL
L	L	AI → A
L	H	$\overline{AI}$ → A
H	L	WR → A
H	H	$\overline{WR}$ → A

B-SOURCE SEL

B2	B1	B0	SEL
L	L	L	BI → B
L	L	H	$\overline{BI}$ → B
L	H	L	WR → B*
L	H	H	$\overline{WR}$ → B*
H	L	L	XWR → B*
H	L	H	$\overline{XWR}$ → B*
H	H	L	PC → B*
H	H	H	$\overline{PC}$ → B*

REG DESTINATION SEL

S1	S0	SEL
L	L	Σ' → WR
L	H	Σ' → XWR
H	L	Σ' → PC
H	H	Σ' ONLY

*BI/O CAN BE USED AS OUTPUT.

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT*
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR

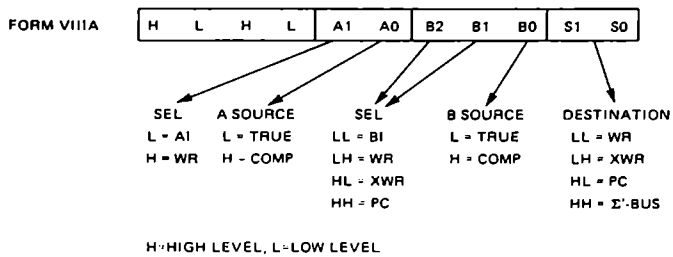
H = HIGH LEVEL, L = LOW LEVEL

1. $\overline{OVFL}$ = LOW
2. $\overline{COUT}$ = $\overline{CIN}$
3. MAGNITUDE: The Σ Bus is compared to ZERO. Resultant outputs are:
   - AG = H (Σ Bus Arithmetically > ZERO)
   - LG = H (Σ Bus > ZERO)
   - EQ = H (Σ Bus = ZERO)

FIGURE 29 – FORM VIII–LOGICAL OPERATIONS: A { NOR / OR / X-OR } B → REGISTER

3.9.1 NOR/AND Logical Operations

Operation Form VIIIA can be used to perform the NOR or AND logical combination of two selectable operands and route the results to one of four destinations. The operation microcode is:



H=HIGH LEVEL, L=LOW LEVEL

As shown above, the A and B sources are selectable by the A1, B1, and B2 bits in their true or complementary form (bits A0, B0) to facilitate performing the NOR, mixed NOR/AND, and the AND functions. As implemented, see Figure 30, the NOR function is performed when the sources are both true, mixed NOR/AND functions are performed with one source complemented, and the AND function is performed when both sources are selected in their complement form. Both implementation and other/equal logic symbols are shown in Figure 30. Also provided are the function tables and Boolean equations.

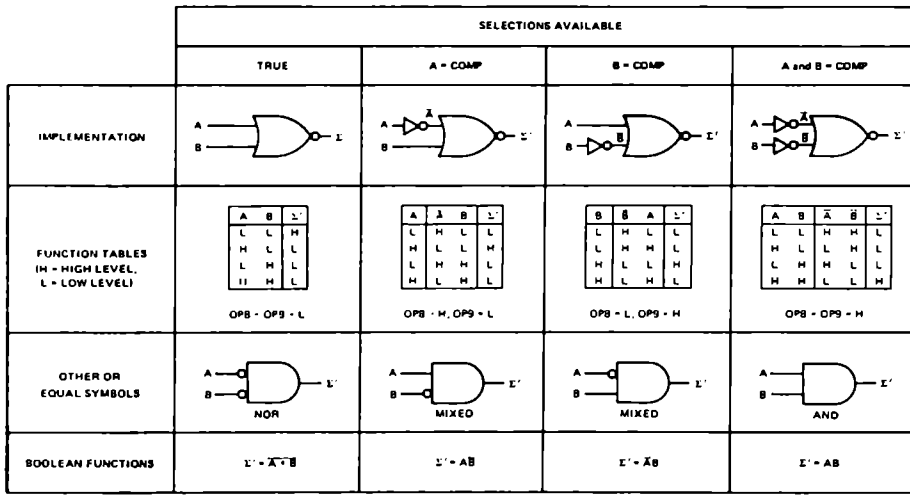
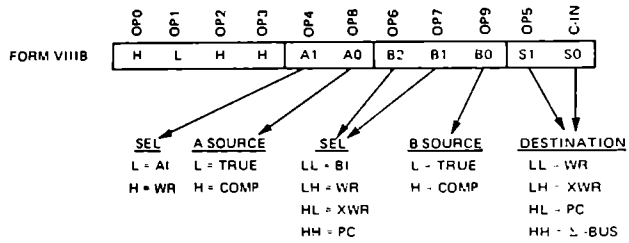


FIGURE 30 – FORM VIIIA NOR/AND LOGICAL OPERATIONS

3.9.2 OR/NAND Logical Operations

Operation Form VIIIB can be used to perform the OR or NAND logical combination of two selectable operands and route the results to one of four destinations. The operation microcode is:



H=HIGH LEVEL, L=LOW LEVEL

As shown above, the A and B sources are selectable by the A1, B1, and B2 bits in their true or complementary form (bits A0, B0) to facilitate performing the OR, mixed OR/NAND, and the NAND functions. As implemented, see Figure 31, the OR function is performed when the sources are both true, mixed OR/NAND functions are performed with one source complemented, and the NAND function is performed when both sources are selected in their complement form. Both implementation and other/equal logic symbols are shown in Figure 31. Also provided are the function tables and Boolean equations.

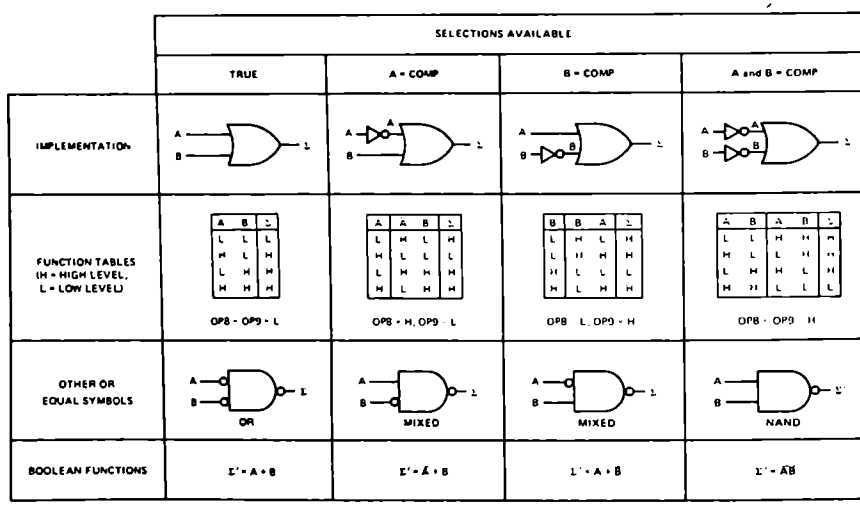
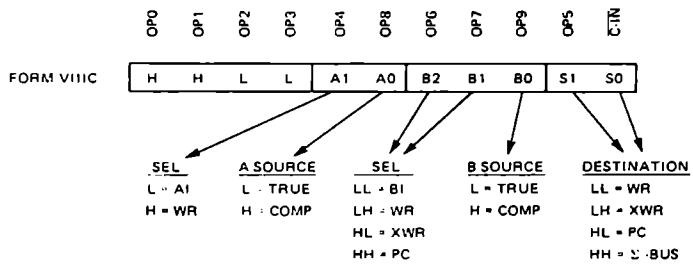


FIGURE 31 – FORM VIIIB OR/NAND LOGICAL OPERATIONS

3.9.3 Exclusive-OR/Exclusive-NOR Logical Operations

Operation Form VIIIC can be used to perform the exclusive-OR/exclusive-NOR logical combination of two selectable operands and route the results to one of four destinations. The operation microcode is:



H = HIGH LEVEL, L = LOW LEVEL

As shown above, the A and B sources are selectable by the A1, B1, and B2 bits in their true or complementary form (bits A0, B0) to facilitate both exclusive-OR and exclusive-NOR operations. As implemented, see Figure 32, the exclusive-NOR function is performed when the sources are both true or both complemented. When either the A or the B source (not both) are complemented, the exclusive-OR function is performed. Both implementation and other/equal logic symbols are shown in Figure 32. Also provided are the function tables and Boolean equations.

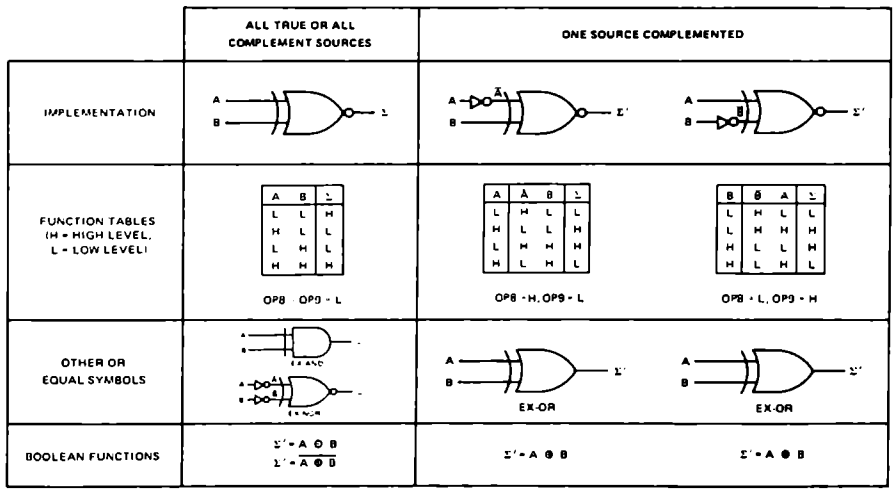

ALL TRUE OR ALL COMPLEMENT SOURCES
ONE SOURCE COMPLEMENTED
IMPLEMENTATION
FUNCTION TABLES (H = HIGH LEVEL, L = LOW LEVEL)
OP8 = OP9 = L
OP8 = H, OP9 = L
OP8 = L, OP9 = H
OTHER OR EQUAL SYMBOLS
EX-OR
EX-OR
BOOLEAN FUNCTIONS
Σ' = A ⊕ B
Σ' = A ⊕ B
Σ' = A ⊕ B

FIGURE 32 – FORM VIIIC EXCLUSIVE-OR/EXCLUSIVE-NOR OPERATIONS

3.10 OPERATION FORM IX – NO OP

Operation Form IX is designed specifically to clear the Σ' bus force AG and LG low, and force EQ high; and, during this operation form data in the 'S481 registers, counters and latches remain unchanged unless directed to do otherwise by the asynchronous control inputs as shown in Figure 33.

The memory or program counter can be incremented (by one or two) on each clock transition, or the working register can be loaded on each clock. Additionally, the B input/output can be specified, as well as sources for the address or data out ports. States of the carry and overflow outputs are not interrupted.

OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	OP8	OP9	CIN
H	H	H	H	H	X	X	X	X	X	X

H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

ASYNCHRONOUS CONTROLS:

SEL B INPUT/OUTPUT
SEL DOB SOURCE
SEL AOB SOURCE
INCREMENT PC OR MC
INHIBIT PC AND/OR MC
LOAD WR

AG = ZERO
LG = ZERO
EQ = HIGH

FIGURE 33 – FORM IX–NO OPERATION: ZERO → Σ' BUS

3.11 OPERATION FORM X – CYCLIC REDUNDANCY CHARACTER ACCUMULATION

Operation Form X is a macroinstruction which can be used to update a 16-bit cyclic redundancy character (CRC) partial sum in eight clock cycles, assuming 8-bit data characters. The updated CRC partial sum resides in the working register. The flow diagram of this algorithm is illustrated in Figure 34.

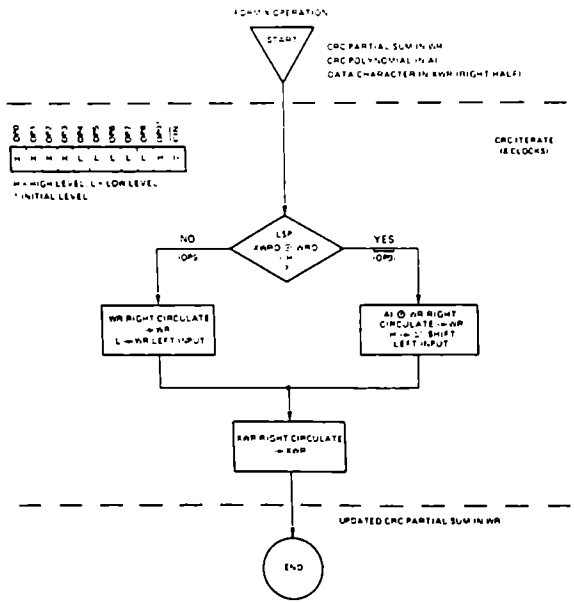


FIGURE 34 – CYCLIC REDUNDANCY CHARACTER ACCUMULATION

Setup conditions include the existence or placement of the previous CRC partial sum in the working register, the CRC polynomial at the A input port, and the data character in the eight least significant bits of the extended working register. All decisions after setup are decoded on chip for each of the eight iterations. Microcontrol open-collector output OP9 of the LSP assumes control during the iterations to generate one of two microinstructions requires to accomplish the CRC update.

3.12 OPERATION FORM XI – SIGNED INTEGER DIVIDE

Operation Form XI consists of the micro/macroinstructions needed to perform the signed division of a double length dividend by an N-bit divisor in N + 3 clock times. After the division routine the quotient will reside in the extended working register (XWR) and the remainder will be in the working register (WR). Negative results are in two's complement. The flow diagram of this algorithm is illustrated in Figure 35.

Setup conditions include the existence or placement of the double length dividend in the WR, XWR and application of the divisor at the A input port. To obtain a legitimate result, the divisor must not be arithmetically zero as indicated during the start command by the EQ output being low. The dividend must be of a nature that it could be generated by a signed multiply and add operation on the divisor. Status outputs LG, AG, C-OUT and OV are undefined, as is EQ after the start command.

After setup, all decisions are decoded on chip for start, iterate, iteration finish, fix remainder, and adjust quotient. The iterate macroinstruction (Form XIB) internally decodes the status of the stored signs, carry out, and working register and the OP8 and OP9 microcontrol open-collector outputs of the MSP assume control generating one of four microinstructions required to accomplish the signed divide.

3.13 OPERATION FORM XII – UNSIGNED DIVIDE

Operation Form XII consists of micro/macroinstructions needed to perform the unsigned division of a double length dividend by an N-bit divisor in N + 1 clock times. After the division routine the binary magnitude quotient will reside in the extended working register (XWR) and the binary magnitude remainder will be in the working register (WR). The flow diagram of this algorithm is illustrated in Figure 36.

Setup conditions include the existence or placement of the double length dividend in the WR, XWR; application of the divisor at the A input port and that the last operation was not a divide command. To obtain a legitimate result, the N-bit divisor must be logically greater than the most-significant N-bits resident in the working register. A direct status on the arithmetically-greater-than (AG) output indicates that a valid (start) [AG = H], or invalid (abort) [AG = L] setup condition exists.

After setup, all decisions are decoded on chip for start, iterate and finish. The iterate macroinstruction (Form XIIB) internally decodes the status of C-OUT or FORCE LOAD FLAG and the OP9 microcontrol open-collector output of the MSP assumes control generating one of two microinstructions required to accomplish the unsigned divide.

3.14 OPERATION FORM XIII – UNSIGNED MULTIPLY

Operation Form XIII consists of a macroinstruction which performs the unsigned multiplication of two N-bit words in N clock times. After the multiply routine the double length product is residing in the working register (most-significant N-bits) and the extended working register (least-significant N-bits). The flow diagram of this algorithm is illustrated in Figure 37.

Setup conditions include clearing the working register to all zeros, loading (not shifting) the multiplier into the extended working register, and applying the multiplicand at the A input port. Arithmetic shift commands must not occur between multiplier load and the first iteration. Status outputs (EQ, AG, LG, C-OUT and OV) are undefined during this algorithm.

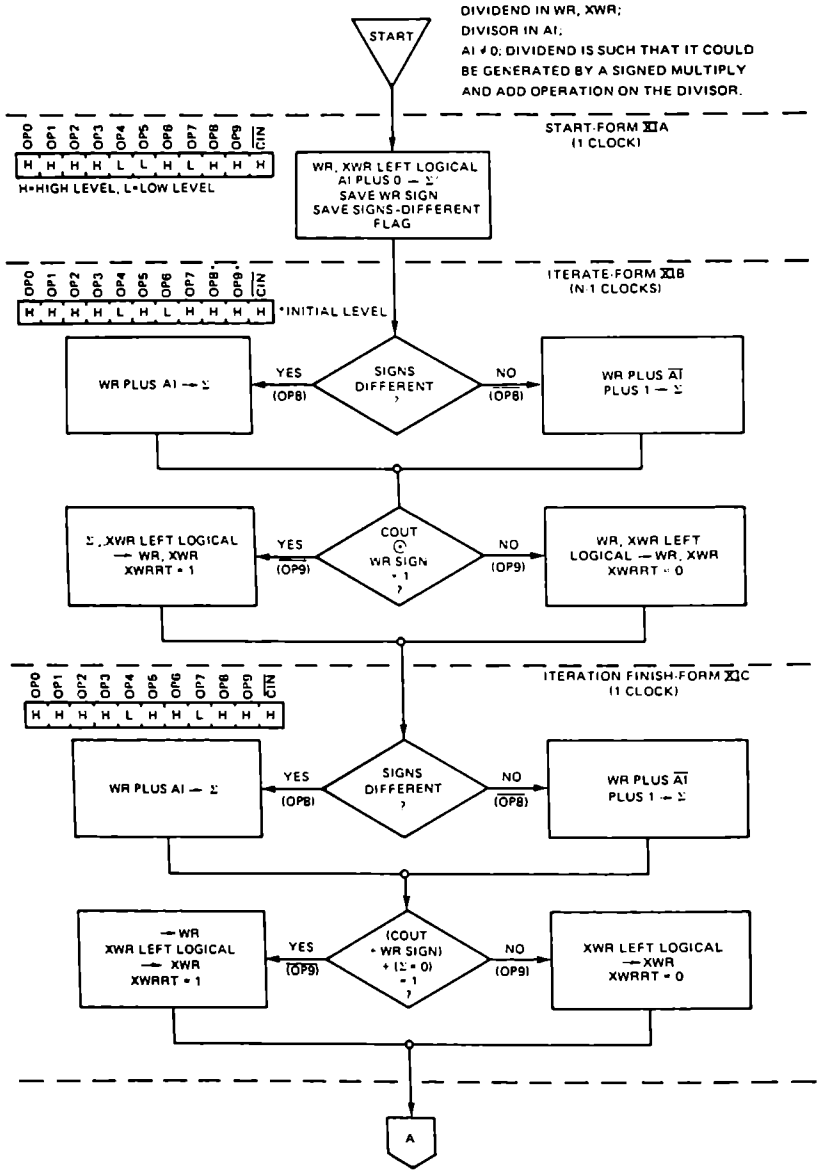

START
DIVIDEND IN WR, XWR;
DIVISOR IN AI;
AI ≠ 0; DIVIDEND IS SUCH THAT IT COULD BE GENERATED BY A SIGNED MULTIPLY AND ADD OPERATION ON THE DIVISOR.
START-FORM XIA (1 CLOCK)
OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7 OP8 OP9 CIN
H H H H L L H L H H H
H=HIGH LEVEL, L=LOW LEVEL
WR, XWR LEFT LOGICAL
AI PLUS 0 → Σ
SAVE WR SIGN
SAVE SIGNS-DIFFERENT FLAG
ITERATE-FORM XI8 (N-1 CLOCKS)
OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7 OP8* OP9* CIN
H H H H L H L H H H H
*INITIAL LEVEL
WR PLUS AI → Σ
YES (OP8)
SIGNS DIFFERENT ?
NO (OP8)
WR PLUS AI PLUS 1 → Σ
Σ, XWR LEFT LOGICAL → WR, XWR
XWRT = 1
YES (OP9)
COUT ⊙ WR SIGN = 1 ?
NO (OP9)
WR, XWR LEFT LOGICAL → WR, XWR
XWRT = 0
ITERATION FINISH-FORM XIC (1 CLOCK)
OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7 OP8 OP9 CIN
H H H H L H H L H H H
WR PLUS AI → Σ
YES (OP8)
SIGNS DIFFERENT ?
NO (OP8)
WR PLUS AI PLUS 1 → Σ
→ WR
XWR LEFT LOGICAL → XWR
XWRT = 1
YES (OP9)
(COUT = WR SIGN) + (Σ = 0) = 1 ?
NO (OP9)
XWR LEFT LOGICAL → XWR
XWRT = 0
A

FIGURE 35 – FORM XI–SIGNED INTEGER DIVIDE (SHEET 1 OF 2)

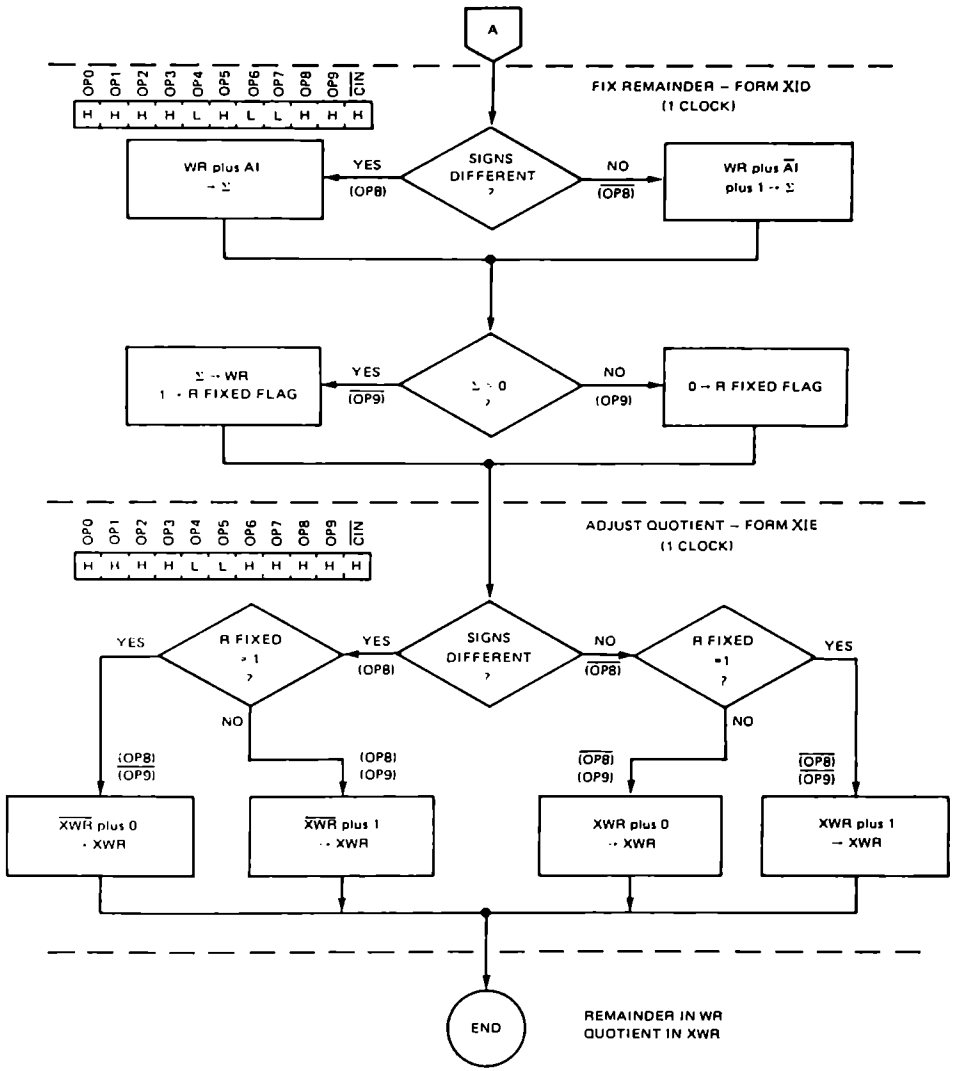


FIGURE 35 – FORM XI–SIGNED INTEGER DIVIDE (SHEET 2 OF 2)

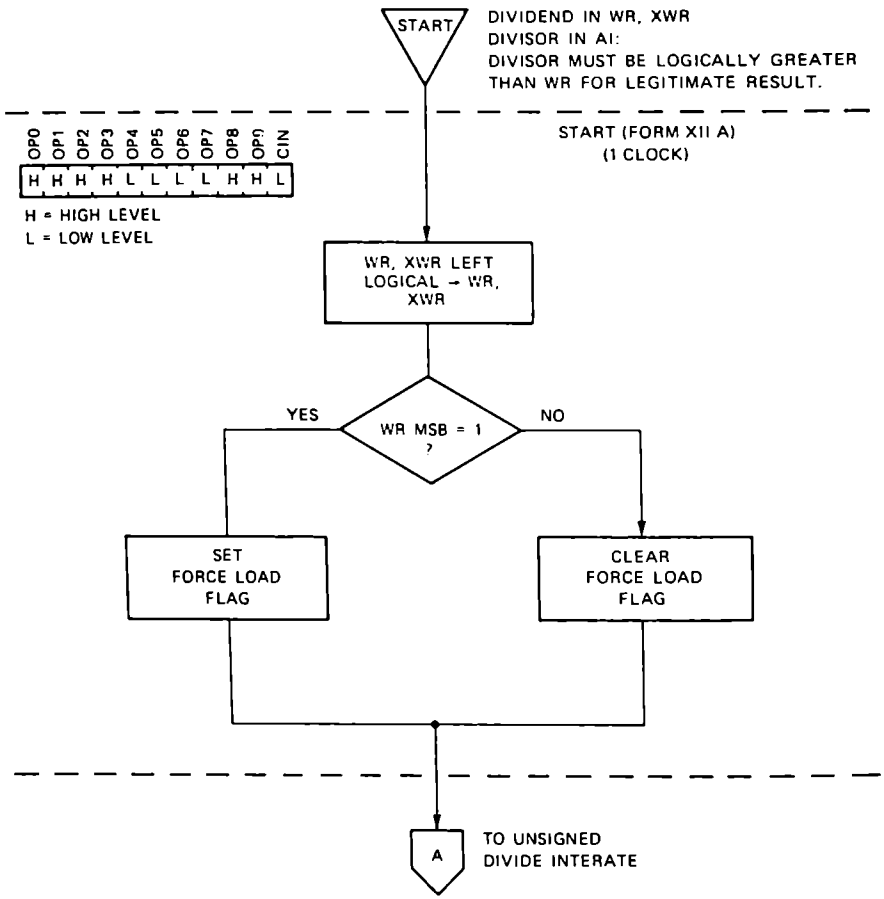


FIGURE 36 – FORM XII–UNSIGNED DIVIDE (SHEET 1 OF 2)

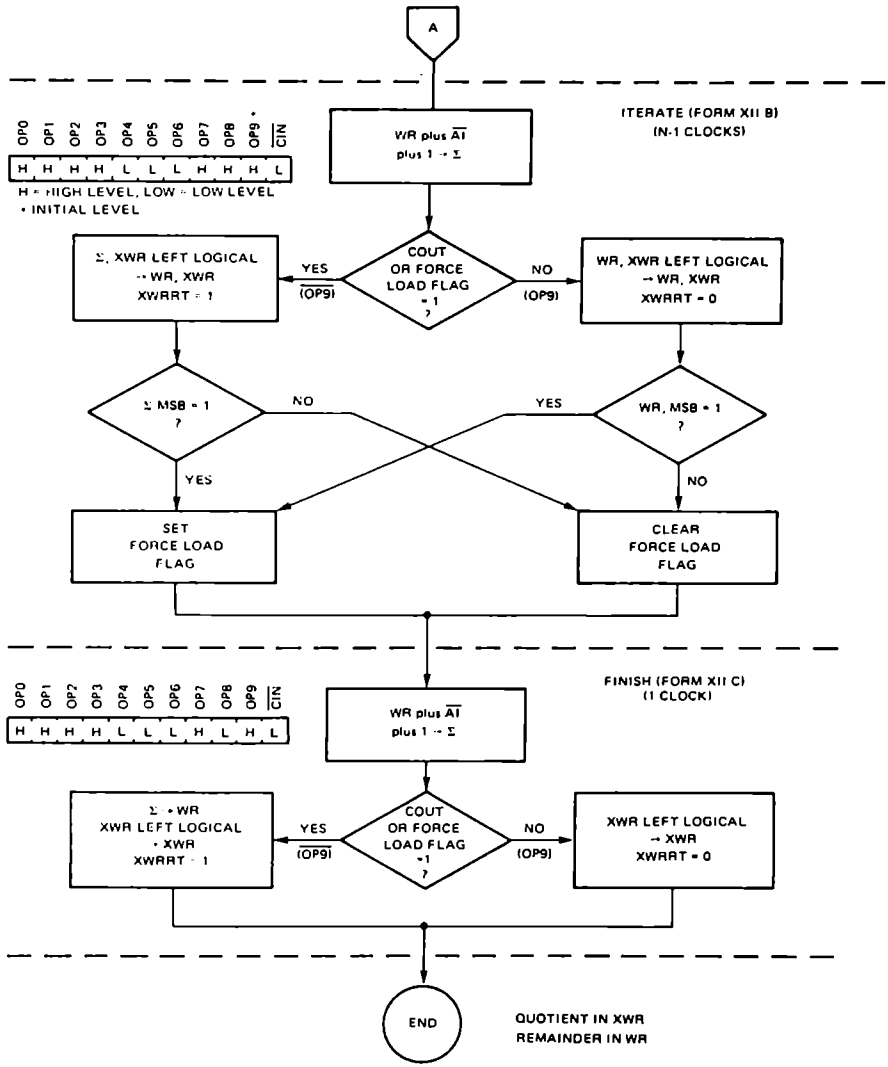

A
ITERATE (FORM XII B)
(N-1 CLOCKS)
OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7 OP8 OP9* CIN
H H H H L L L H H H L
H = HIGH LEVEL, LOW = LOW LEVEL
* INITIAL LEVEL
WR plus AI plus 1 → Σ
COUT OR FORCE LOAD FLAG = 1 ?
YES (OP9)
NO (OP9)
Σ, XWR LEFT LOGICAL → WR, XWR XWRRT = 1
WR, XWR LEFT LOGICAL → WR, XWR XWRRT = 0
Σ MSB = 1 ?
WR, MSB = 1 ?
NO
YES
YES
NO
SET FORCE LOAD FLAG
CLEAR FORCE LOAD FLAG
FINISH (FORM XII C)
(1 CLOCK)
OP0 OP1 OP2 OP3 OP4 OP5 OP6 OP7 OP8 OP9 CIN
H H H H L L L H L H L
WR plus AI plus 1 → Σ
COUT OR FORCE LOAD FLAG = 1 ?
YES (OP9)
NO (OP9)
Σ → WR XWR LEFT LOGICAL → XWR XWRRT = 1
XWR LEFT LOGICAL → XWR XWRRT = 0
END
QUOTIENT IN XWR
REMAINDER IN WR

FIGURE 36 – FORM XII–UNSIGNED DIVIDE (SHEET 2 OF 2)

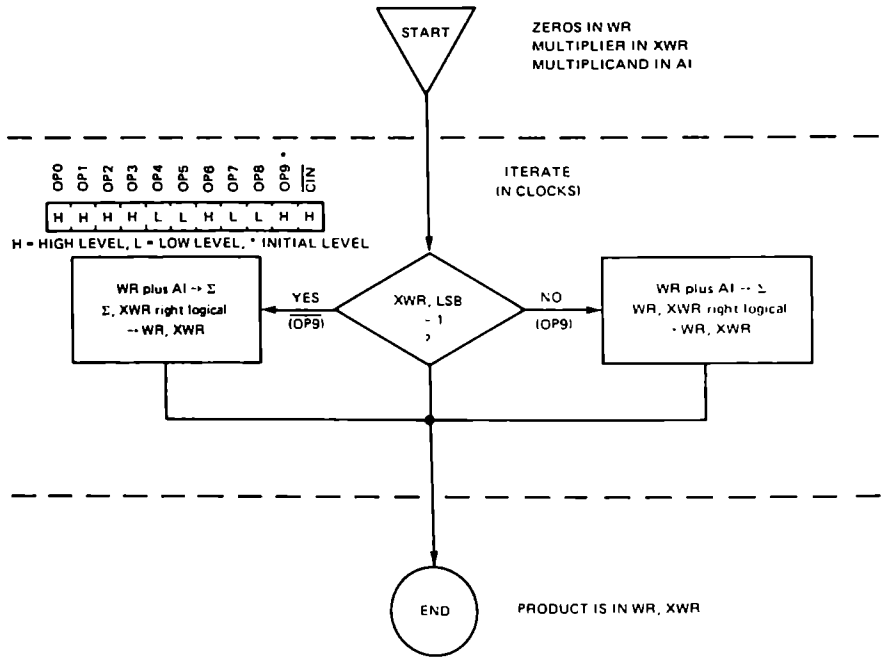


FIGURE 37 – FORM XIII–UNSIGNED MULTIPLY

The iterate macroinstruction internally decodes the status of the XWR LSB and the OP9 microcontrol open collector output of the MSP assumes control generating one of two microinstructions required to accomplish the unsigned multiply.

3.15 OPERATION FORM XIV – SIGNED INTEGER MULTIPLY

Operation Form XIV consists of a macroinstruction which performs the signed multiplication of two N-bit signed integers in N clock times. After the multiply routine, the double precision signed product resides in the working register (most-significant N-bits) and the extended working register (least-significant N-bits). Negative products are in two's complement. The flow diagram of this algorithm is illustrated in Figure 38.

Setup conditions include clearing the working register to all zeros, loading (not shifting) the multiplier into the extended working register, and applying the multiplicand at the A input port. Arithmetic shifts must not occur between multiplier load and the first iteration. Status outputs (EO, AG, LG, C-OUT, and OV) are undefined during this algorithm.

The iterate macroinstruction internally decodes the status of the multiplier (XWR) sign-bit flag, the multiplier LSB, and the multiplier LSB flag and the OP8 and OP9 microcontrol open-collector outputs of the MSP assume control generating one of four microinstructions required to accomplish the signed multiply.

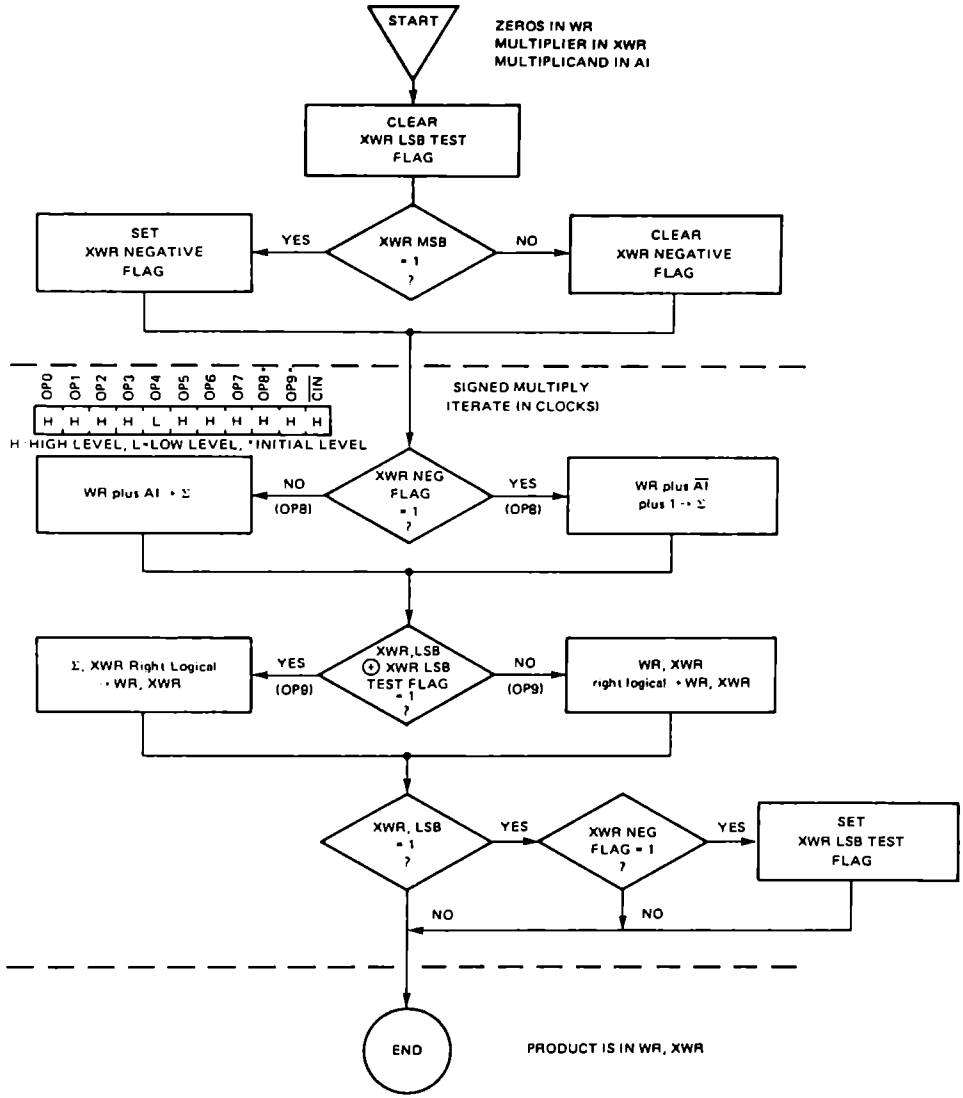


FIGURE 38 – FORM XIV–SIGNED INTEGER MULTIPLY

4. SPECIFICATIONS

Recommended operating conditions, electrical characteristics, and switching characteristics are provided in Tables 19 through 21.

TABLE 19
RECOMMENDED OPERATING CONDITIONS

		SN54S481			SN74S481			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.75	V
High-level output voltage at EQ, OP8, OP9				5.5			5.5	V
Low-level output current	AOP, BI/O, DOP, $\overline{CCO}$/OV, $\overline{COUT}$			10			10	mA
	EQ, OP8, OP9			8			8	
	WRLFT, WRRT, XWRLFT, XWRRT			4			4	
	X/LG, Y/AG			20			20	
High-level output current	BI/O, DOP			2			6.5	mA
	All other outputs or I/O except EQ, OP8, OP9			1			1	
Width of clock pulse	High logic level	35			25			ns
	Low logic level	50			35			
Clock frequency				7.5			10	MHz
Setup time, t_{su}	AI, BI/O → Latch	0↕			0↕			ns
	AI → WR	35↑			25↑			
	AI, BI/O → ALU → MC, PC, WR, XWR	80↑			65↑			
	$\overline{CCI}$, $\overline{INCMC}$, $\overline{INCPC}$, $\overline{LDWR}$	55↑			45↑			
	OP0 thru OP9	80↑			70↑			
Hold time, t_h	AI, BI/O → Latch	20↕			15↕			ns
	AI → WR	10↑			10↑			
	AI, BI/O → ALU → MC, PC, WR, XWR	0↑			0↑			
	$\overline{CCI}$, $\overline{INCMC}$, $\overline{INCPC}$, $\overline{LDWR}$	0↑			0↑			
	OP0 thru OP9	$t_{w(clock)}$			$t_{w(clock)}$			
Operating free-air temperature range, T_A		−55	25	125	0	25	70	C

↑↓The arrow indicates the transition of the clock input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition

DESIGN GOAL
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

TABLE 20

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	54S'	2.5	3.4		V
				74S'	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	POS	V_{CC} = MAX, V_I = V_{CC}				1	mA
		OP0, OP1, OP2, OP3, $\overline{CIN}$	V_{CC} = MAX, V_I = 2.7 V				200	μA
		Any other					100	
I_{IL}	Low-level input current	OP0, OP1, OP2 OP3, $\overline{CIN}$	V_{CC} = MAX, V_I = 0.5 V				−3.2	mA
		WRRT, WRLFT, XWRRT, XWRLFT, $\overline{CCI}$, CLOCK					−2	
		Any other					−1	
I_{OS}	Short-circuit output current§	Any output or I/O except EQ, OP8, OP9	V_{CC} = MAX		−30		−100	mA
I_{CC}	Supply current		V_{CC} = MAX			225		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

TABLE 21

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

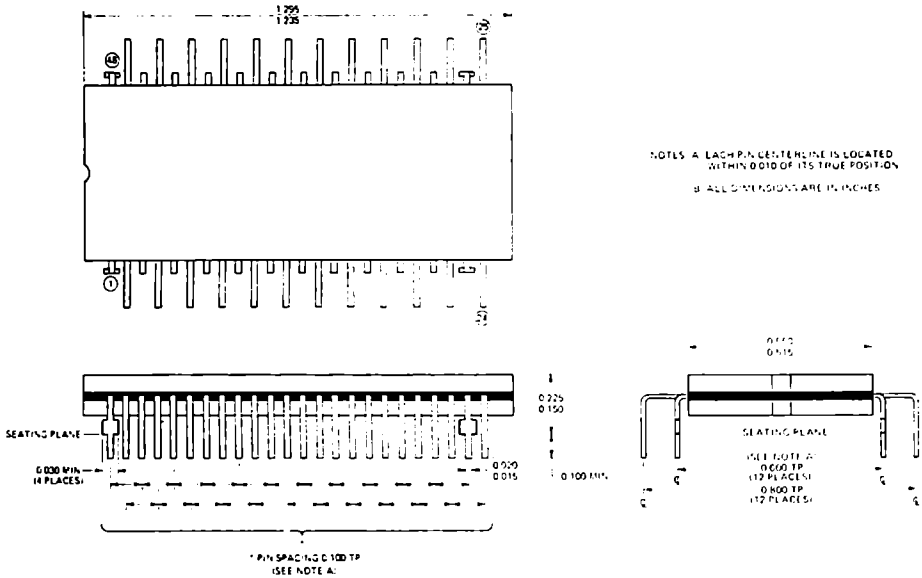
PARAMETER	FROM (INPUT)	TO (OUTPUT)	OPERATION ROUTING	MIN	TYP	MAX	UNIT
t_p	AI, BI/O	DOP	LATCH → ALU → DOP		80		ns
		WRLFT, WRRT	LATCH → ALU		80		ns
		Y/AG, X/LG, $\overline{COUT}$	LATCH → ALU		60		ns
		EQ, OV	LATCH → ALU		60		ns
t_p	AI, BI/O	BI/O	LATCH → ALU		90		ns
t_p	$\overline{CIN}$	$\overline{COUT}$			20		ns
t_p	$\overline{CCI}$	$\overline{CCO}$			15		ns
t_p	A0	AOP			20		ns
t_p	D0, D1	DOP			20		ns
t_{PXZ}	BI/O SEL or D0, D1	BI/O or DOP			10		ns
t_{PZX}	BI/O SEL or D0, D1	BI/O or DOP			15		ns
t_p	CLOCK	AOP, DOP	NO SHIFT		30		ns
		WRLFT, WRRT, XWRLFT, XWRRT	[WR, XWR, Σ-BUS] → SHIFTED		30		ns
		AOP, DOP			30		ns
		AOP, DOP	[WR, XWR, PC] → ALU → SHIFTED		90		ns
		OV			50		ns
		$\overline{CCO}$			25		ns
		$\overline{COUT}$			50		ns
		OP8, OP9			30		ns
t_p	$\overline{CIN}$	DOP			40		ns

t_p = Propagation delay
t_{PXZ} = Disable time to HI-Z
t_{PZX} = Enable time (HI-Z-To-Enable)

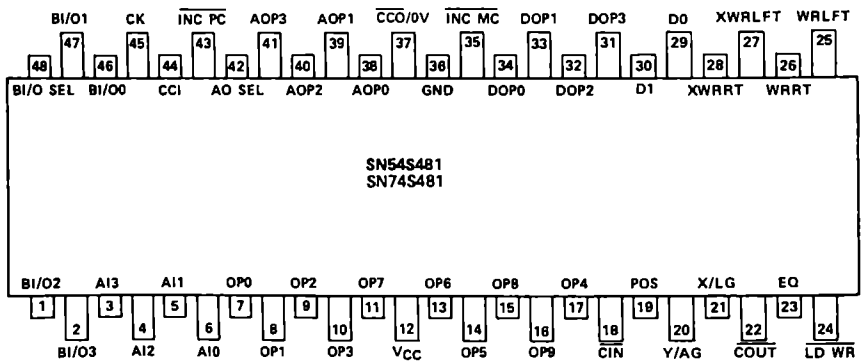
DESIGN GOAL

This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

5. MECHANICAL DATA



6. PIN ASSIGNMENTS


BI/O1 CK INC PC AOP3 AOP1 CCO/0V INC MC DOP1 DOP3 D0 XWRLFT WRLFT
47 45 43 41 39 37 35 33 31 29 27 25
48 46 44 42 40 38 36 34 32 30 28 26
BI/O SEL BI/O0 CCI AO SEL AOP2 AOP0 GND DOP0 DOP2 D1 XWRRT WRRT
SN54S481
SN74S481
BI/O2 AI3 AI1 OP0 OP2 OP7 OP6 OP8 OP4 POS X/LG EQ
1 3 5 7 9 11 13 15 17 19 21 23
2 4 6 8 10 12 14 16 18 20 22 24
BI/O3 AI2 AI0 OP1 OP3 VCC OP5 OP9 CIN Y/AG COUT LD WR

The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

SBP0400A
SBP0401A
4-Bit-Slice
I^2L Processor Elements
Data Manual

OCTOBER 1976

TEXAS INSTRUMENTS
INCORPORATED

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1. INTRODUCTION

The SBP0400A and SBP0401A are 4-bit expandable parallel binary processor elements, each monolithically integrating 1660 functional gates. These controller/processor building blocks combine the unique properties of Integrated Injection Logic (I^2L) with a microprogrammable bit-slice architecture to offer a high degree of performance and design flexibility. Each can provide the basis for efficient, low-cost solutions to a wide range of applications, from basic sequential controllers to advanced multiprocessor systems for either industrial or military environments.

1.1 ARCHITECTURAL FEATURES

Primary among the SBP0400A and SBP0401A architectural features are:

- Microprogrammable, bit-slice design expandable in 4-bit multiples
- Separate data-in, data-out, address-out and control ports provide flexible parallel device access
- 16-function arithmetic/logic unit (ALU) with symmetrical subtraction and fully carry look-ahead capability
- 8-word general register file including program counter with independent incrementor
- Two 4-bit working registers for both single- and double-length operations
- Dual scaled-shifters with on-chip handling of end conditions
- Versatile factory programmable logic array (PLA) generates on-chip control transformation
- The SBP0400A features an on-chip pipelining operation register
- The SBP0401A, with asynchronous microinstruction decode, is designed for use in externally pipelined systems

1.2 OPERATIONAL FEATURES

The functional power of the SBP0400A or SBP0401A is characterized by their ability to perform, within a single clock cycle, any one of a repertoire of 512 standard operations:

- Operand modifications or combinations via eight arithmetic or eight Boolean functions of the ALU
- Double length accumulator with full bidirectional single/double precision arithmetic/logical/circulate shift capabilities, including sign protection
- Single clock ALU/shift combinations simplify implementation of iterative multiple and non-restore divide algorithms
- Special select operations and transfers

1.3 ADDITIONAL FEATURES

When provided with external control for sequencing of its operation set, either an SBP0400A or SBP0401A based system design can efficiently emulate a large number of existing systems with full software compatibility and no loss of software investment. Or complete application-tailoring of custom instructions may be accomplished for any design. Additional features are:

- Independent program counter with independent access controls (and the internal operation register of the SBP0400A) provide instruction look-ahead capability (pipelining)
- Relative position control defines bit-slice rank in N-bit applications

- Serial and parallel access to or from working registers
- Word or byte incrementation of program counter
- ALU bypass for direct register-file access

1.4 TECHNOLOGICAL FEATURES

These processor elements, fabricated with Integrated Injection Logic (I^2L), feature an extremely wide performance range.

- Constant speed-times-power performance over an injector current range covering three orders of magnitude (10^3)
- Operates from a single dc power source capable of 1.1 volt minimum at desired injector current
- ALU/shift operation time . . . 240 nanoseconds typical at 200 mW nominal power
- Fully TTL compatible at nominal injector current
- Static operation with positive (↑) edge-triggered storage
- SBP0400AC and SBP0401AC operate over 0°C to 70°C industrial temperature range
- SBP0400AM and SBP0401AM operate over full −55°C to 125°C military temperature range

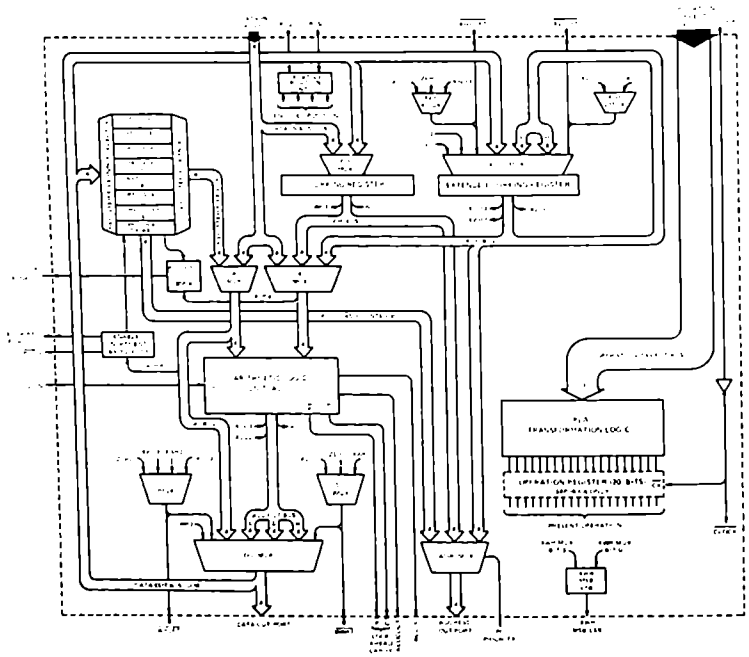


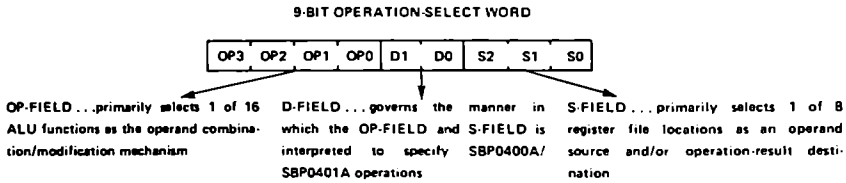
FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM

2. FUNCTIONAL PIN DESCRIPTIONS

PIN NUMBER	PIN NAME	PIN FUNCTION	INPUT, OUTPUT, OR INPUT/OUTPUT
1 2	D1 D0	2-bit, "D" field of the Operation-Select Word.	Input Input
3 4 5	S2 S1 S0	3-bit, "S" field of the Operation-Select Word designates, in general, a particular RF as an operand source/destination.	Input Input Input
6	$\overline{\text{XWRLFT}}$	Bidirectional I/O, low active, shift accommodation for the XWR. Receives double-precision right-shift data; outputs double-precision left-shift data. Becomes XWRLFT (high active) internally.	Bidirectional Input/output
7	$\overline{\text{XWRRT}}$	Bidirectional I/O, low active, shift accommodation. Receives double-precision left-shift data; outputs double-precision right-shift data. Becomes XWRRT (high active) internally.	Bidirectional Input/output
8	XWR MSB/LSB	MSB of the input to the XWR if in the most-significant 4 bit slice position (MSP) and LSB input to the XWR if in the least-significant 4 bit slice position (LSP).	Output
9	$\overline{\text{WRRT}}$	Bidirectional I/O, low-active, shift accommodation for ALU output data. Receives left-shift data. Outputs right-shift data. Becomes WRRT (high active) internally.	Bidirectional Input/output
10	$\overline{\text{WRLFT}}$	Bidirectional I/O, low-active, shift accommodation for ALU output data. Receives right-shift data; outputs left-shift data. Becomes WRLFT (high active) internally.	Bidirectional Input/output
11	ALUCIN	Receives, high-active, ALU ripple carry-in data.	Input
12 13 14 15	DOP0 DOP1 DOP2 DOP3	4-bit, parallel, high active, data-out port. (DOP3 - DOP0)	Output Output Output Output
16 17 24 25	DIP3 DIP2 DIP1 DIP0	4-bit, parallel, high active, data-in port (DIP3 -- DIP0)	Input Input Input Input
18	$\overline{\text{PCCIN}}$	In all positions, directs the program counter to increment by 1 or 2, depending on the level applied to ENINCBY2, on the next low-to-high clock transition.	Input
19	$\overline{\text{PCCOUT}}$/ BMSB	In any position but MSP, PCCOUT is the program counter output applied to the next more significant package $\overline{\text{PCCIN}}$. In the MSP, outputs the MSB of the "B" bus.	Output
20	GND	Common or ground terminal	Supply Common
21 22	POS0 POS1	Directs internal and input/output end-conditions required to define the relative position of each SBP0400A/SBP0401A when a number is cascaded to implement > 4-bit word lengths. See double-precision shift data flow.	Input Input
23	ENINCBY2/ AMSB	In the least-significant 4-bit slice position (LSP), ENINCBY2 = H in conjunction with $\overline{\text{PCCIN}}$ = L directs the PROGRAM COUNTER to increment by a displacement of 2 on the next clock. In the most-significant 4-bit slice position (MSP), outputs the MSB of the "A" bus.	Bidirectional Input/output (LSP) (MSP)
26	CLOCK	Clocks all synchronous registers on positive transition.	Input (Edge-triggered)
27	ALU 0	Active high open-collector output indicates that the four ALU outputs are low (equal zero).	Output
28 29 31 32	AOP3 AOP2 AOP1 AOP0	4-bit, parallel, high-active, address-out port. (AOP3 -- AOP0)	Output Output Output Output
30	PC PRIORITY	Selects program counter to the address-out port (high active). Overrides internal direction of address-out port.	Input
33	$\overline{\text{P}}$	ALU Carry-propagate	Output
34	$\overline{\text{G}}$	ALU Carry-generate	Output
35	ALUCOUT	Outputs, high active, ALU ripple carry-out data.	Output
36 37 38 39	OP3 OP2 OP1 OP0	This 4-bit "OP" field of the Operation-Select Word designates in general, 1 of 16 ALU functions.	Input Input Input Input
40	INJECTOR	Supply current source.	Supply input

3. DETAILED FUNCTIONAL DESCRIPTION

The SBP0400A and SBP0401A architectures are formed by the various functional blocks and interconnecting data/control paths shown in Figure 1. Parallel data/control flow to/from the processor element is accomplished through 1) the data-in port (DIP) via the 4-bit data-in bus (DIB), 2) the data-out port (DOP) via the 4-bit data-out bus (DOB), 3) the address-out port (AOP) via the 4-bit address-out bus (AOB), and 4) the operation-select port (OSP) via the nine operation-select inputs. The format of the op-select word is:


9-BIT OPERATION-SELECT WORD
OP3
OP2
OP1
OP0
D1
D0
S2
S1
S0
OP-FIELD . . . primarily selects 1 of 16 ALU functions as the operand combination/modification mechanism
D-FIELD . . . governs the manner in which the OP-FIELD and S-FIELD is interpreted to specify SBP0400A/SBP0401A operations
S-FIELD . . . primarily selects 1 of 8 register file locations as an operand source and/or operation-result destination

NOTE

A complete discussion of the operation-select word is provided in section 5.

The SBP0400A contains a 20-bit operation register which stores, on the clock positive transition, the present (resident) operation decoded by the transformation PLA. The SBP0401A, containing the identical operation decode 20-output PLA, derives the present (resident) operation from the steady-state input at the nine op-select inputs. The '0401A is designed specifically for use in systems utilizing the SN54S/74S482 control element which, in addition to generating next control-memory addresses and storing interrupt/subroutine addresses, contains an on-chip control memory address register to assist with the system pipelining functions. Thus, the need for an operation register in the SBP0401A processor element is eliminated.

3.1 PROGRAMMABLE LOGIC ARRAY (PLA)

3.1.1 PLA Description

The programmable logic array (PLA) is a factory-programmable block of combinational logic which forms the control operation transformation center. Nine bits of encoded microinstruction data are presented to the PLA via the 9-bit operation-select word input lines. The PLA decodes/translates this encoded data to generate a 20-bit internal microinstruction. The various micro-operation fields of this microinstruction condition the appropriate functional blocks and buses for microinstruction execution.

On the positive going (↑) transition at the clock input, this 20-bit microinstruction is stored in the operation register (OR) of the SBP0400A.

3.1.2 PLA Factory Programming

The standard factory PLA program provides a flexible, universal, repertoire of 459 unique operations. However, the PLA can be factory programmed to provide, within the constraint of 62 AND terms and 20 OR terms, a personality tailored to meet custom requirements.

3.2 SBP0400A OPERATION REGISTER (OR)

The 20-bit operation register (OR) of the SBP0400A is a D-type edge-triggered register which, on each positive transition at the clock input, loads the present PLA output. The OR, as loaded, continuously enables the various

'0400A functional blocks for execution of the "present" microinstruction while the PLA may be simultaneously decoding/translating the "next" microinstruction.

3.3 STATUS OUTPUTS

Status outputs for the operation in process are designed specifically to simplify system implementation by providing direct access to those status bits used with the classical and highly efficient multiply and divide algorithms. The status outputs consist of:

a. AMSB and BMSB – In the MSP these outputs provide direct access to the sign bits of data/operands entering the ALU.

b. XWR MUX MSB – In the MSP this output provides direct access to the data bit which can become the XWR sign bit during left-shift operations. It is useful for determining overflow (impending change of the XWR sign bit) in double-signed arithmetic operations, shifting operations, or fix-up routines in iterative sign-magnitude divide algorithms.

c. XWR MUX LSB – In the LSP this output provides direct access to the data bit which can become the XWR LSB during right-shift operations. It is useful for looking ahead during iterative multiply and divide routines to setup the next micro-operation.

d. ALU = 0 – In the LSP, IP, and MSP this output provides a direct indication that all four of the ALU outputs are low. In an expanded word length system all of the ALU = 0 outputs can be dot-AND connected to provide, on a single-line, an indication that all of the ALU outputs are low (equal zero).

e. ALUCOUT – In the LSP, IP, and MSP this output provides a direct carry out from each of the 4-bit slices. In the MSP the ALUCOUT can be used for determining ALU overflow.

3.4 ARITHMETIC/LOGIC UNIT (ALU) DESCRIPTION

The 4-bit parallel, binary, arithmetic/logic unit (ALU) is the operand combination/modification mechanism. Under direction of the present micro-operation, the ALU performs 1 of 16 arithmetic/Boolean operations on either or both of two operands present at it's A and B input ports. Operand sources which may access the A input port of the ALU via the A multiplexer are the register file (RF) and data-in port (DIP); operand sources which may access the B input port of the ALU via the B multiplexer are the data-in port (DIP), working register (WR), and extended working register (XWR).

3.4.1 ALU Function Selection

In general, an ALU function is specified via the 4-bit OP-field (OP3 → OP0) of the operation-select word as shown in Table 1. This field is presented to the PLA via the operation-select word input lines. The PLA translates OP3, OP2, OP1, OP0 into a 4-bit micro-operation field which ultimately selects the ALU mode. The OP3 bit functions similarly to an ALU mode control in that 1) a low-logic level places the ALU in an arithmetic mode, and 2) a high-logic level places the ALU in a logic mode. OP2 → OP0 selects a particular function within the specified ALU mode.

3.4.2 ALU Arithmetic Mode

Functionally similar to the popular TTL ALU's, such as the SN54S/74S181 and SN54S/74S281, the arithmetic functions (see Table 1) include symmetrical subtraction whereby either A minus B or B minus A may be employed to simplify data flow. Other arithmetic-type functions include simple A plus B, A plus B plus carry-in, preset all high, clear all low, and direct symmetrical generation of complements (1's or 2's) for either A or B.

TABLE 1
ALU FUNCTION-SELECT TABLE

	ALU OP-FIELD				ACTIVE-HIGH DATA	
	OP3	OP2	OP1	OP0	ALUCIN = H (WITH CARRY, NO BORROW)	ALUCIN = L (WITH CARRY, NO BORROW)
Arithmetic	L	L	L	L	Fn = L	Fn = H
	L	L	L	H	Fn = B minus A	Fn = B minus A minus 1
	L	L	H	L	Fn = A minus B	Fn = A minus B minus 1
	L	L	H	H	Fn = A plus B plus 1	Fn = A plus B
	L	H	L	L	Fn = B plus 1	Fn = B
	L	H	L	H	Fn = $\overline{B}$ plus 1	Fn = $\overline{B}$
	L	H	H	L	Fn = A plus 1	Fn = A
	L	H	H	H	Fn = $\overline{A}$ plus 1	Fn = $\overline{A}$
Logic	H	L	L	L	Fn = AnBn	
	H	L	L	H	Fn = An⊕Bn	
	H	L	H	L	Fn = $\overline{An \oplus Bn}$	
	H	L	H	H	Fn = $\overline{A}$nBn	
	H	H	L	L	Fn = An$\overline{B}$n	
	H	H	L	H	Fn = An + $\overline{B}$n	
	H	H	H	L	Fn = $\overline{A}$n + Bn	
	H	H	H	H	Fn = An + Bn	

3.4.3 ALU Logical (Boolean) Mode

Functionally similar to the popular ALUs such as the SN54S/74S181 and SN54S/74S281, the ALU logical functions (see Table 1) include AND, OR, exclusive OR, exclusive NOR, and four symmetrical mixed combinational functions of the ALU's A and B operands.

3.4.4 ALU Carry and Look-Ahead Generator Functions

These processor elements have accommodations for ALU ripple carry-in (ALUCIN) and ALU ripple carry-out (ALUCOUT); and in order to facilitate look-ahead carry generation across expanded word sizes, each has output accommodations for ALU carry-generate data ($\overline{G}$) and ALU carry-propagate data ($\overline{P}$). When these accommodations are utilized in conjunction with SN54/74182 look-ahead carry generators, ALU add/subtract times may be significantly improved over those times where only ripple-carry techniques are employed. Only one SN54/74182 (Figure 2) is required to provide look-ahead carry generation across an expanded system of from two to four 4-bit slice processor elements. A second level of look-ahead carry generation may be employed (Figure 3) for systems expanded up to 64 bits. Typical ALU add times are shown in Table 2, and are illustrated in Figure 4.

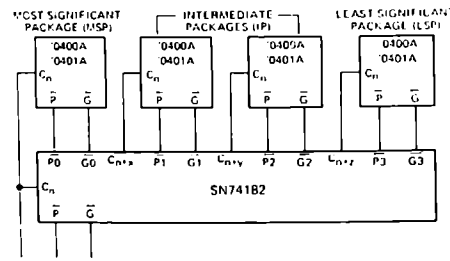


FIGURE 2 – SINGLE-LEVEL ALU CARRY LOOK-AHEAD AND BIT-SLICE RELATIVE POSITIONS

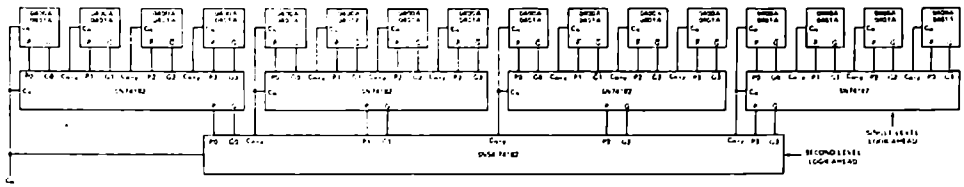


FIGURE 3 – 64-BIT SYSTEM WITH ALU FULL-CARRY LOOK-AHEAD

TABLE 2

TYPICAL SBP0400A ADD TIMES (DIP PLUS WR) FROM ↑ CLOCK TO DO8

TYPE OF CARRY	TWO 4-BIT WORDS	TWO 8-BIT WORDS	TWO 16-BIT WORDS	TWO 32-BIT WORDS	TWO 64-BIT WORDS
RIPPLE	240 ns	285 ns	405 ns	645 ns	1.1 µs
SINGLE-LEVEL LOOK-AHEAD*	NA	300 ns	300 ns	405 ns	525 ns
SECOND-LEVEL LOOK-AHEAD*	NA	NA	NA	315 ns	315 ns

*LOOK-AHEAD IS SN54/74182, AND INJECTOR CURRENT IS 200 mA.

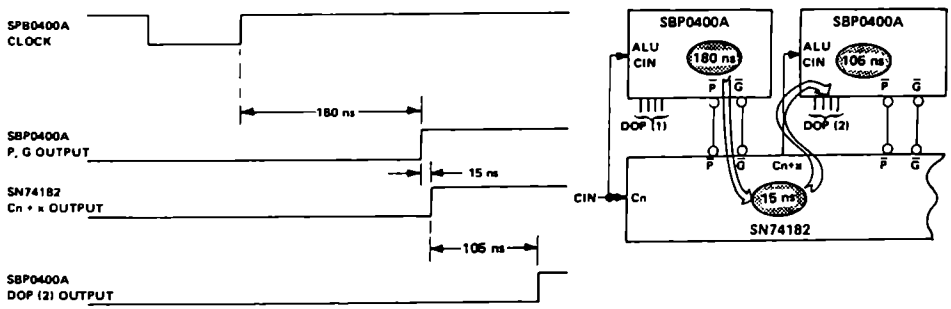


FIGURE 4 – EXECUTION OF TYPICAL ALU MICRO-OPERATION

3.5 RELATIVE POSITION CONTROL (POS1, POS0)

The 2-bit relative position control (POS1, POS0) encodes the relative positional rank of each individual processor element in an expanded word length system. As shown in Figure 2, the three positional rank possibilities are: 1) most significant position/package (MSP), 2) intermediate position/package (IP), and 3) least significant position/package (LSP).

Consequent to encoded positional rank, the relative position control (POS1, POS0), as shown in Table 3 dictates for each individual 4-bit slice in an expanded word length system: 1) the manner in which data shifts/circulates are to be accomplished, and 2) a particular assignment for each individual multifunction I/O accommodation.

TABLE 3
POSITION CONTROL FUNCTIONS

INPUTS		RELATIVE POSITION	MULTIFUNCTION I/O		
POS1	POS0		$\overline{PCCOUT}$/ BMSB	ENINCBY2/ AMSB	XWR MUX MSB/LSB
L	H	LEAST SIGNIFICANT POSITION (LSP)	$\overline{PCCOUT}$	ENINCBY2	XWR LSB
L	L	INTERMEDIATE POSITION (IP)	$\overline{PCCOUT}$	Hi-Z	ZERO
H	L	MOST SIGNIFICANT POSITION (MSP); DOUBLE-SIGNED/DOUBLE-PRECISION (DS/DP) ARITHMETIC SHIFTS	BMSB	AMSB	XWR MSB
H	H	MOST SIGNIFICANT POSITION (MSP); SINGLE-SIGNED/DOUBLE-PRECISION (SS/DP) ARITHMETIC SHIFTS	BMSB	AMSB	XWR MSB

3.6 REGISTER FILE (RF0 → RF7)

3.6.1 RF General Description

The register file (RF) is an 8-word by 4-bit set of D-type edge-triggered registers. Any one of the eight registers may be selected as an operand source and/or operation-result destination. Register selection is accomplished via the 3-bit, S-field (S2 → S0) of the operation-select word. This field is presented to the PLA via the operation-select word input lines. The PLA translates S2, S1, S0 into a 3-bit micro-operation field which ultimately selects a particular register within the file.

3.6.2 RF Source/Destination Operands

Register file source and destination operands are listed in Tables 4 and 5 respectively. When the register file is used as a destination, the source data is recognized only when a low-level condition exists at the clock input. As shown in Figure 5, source data can change during the low-level clock condition as long as the setup time prior to the low-to-high transition of the clock input is satisfied.

TABLE 4
RF SOURCE OPERANDS

OPERATION	OP FORM	OP-FIELD OP3 → OP0	D-FIELD D1 → D0	S-FIELD S2 → S0
RF → DOP	IIIb	LLLL	HL	LLL → HHH
RF → XWR	IIIc	LLLH	HL	LLL → HHH
RF ALU WR → RF	Ia	LLLL → HHHH	LL	LLL → HHH
RF ALU WR → WR	Ib	LLLL → HHHH	LH	LLL → HHH
RF plus DIP plus ALUCIN → RF	IId	LHHH	HL	LLL → HHH
RF plus DIP plus ALUCIN → WR	IIb	LHLL	HL	LLL → HHH
RF plus DIP plus ALUCIN → XWR	IIc	LHLH	HL	LLL → HHH
(RF plus WR plus ALUCIN,XWR) LCIR → WR,XWR	IVd	HLLH	HL	LLL → HHH
(RF plus WR plus ALUCIN,XWR) RSA → WR,XWR	IVi	HLHH	HL	LLL → HHH
RF plus WR plus ALUCIN → XWR	IIa	LLHH	HL	LLL → HHH
RF plus XWR plus ALUCIN → WR	IIe	HHLL	HL	LLL → HHH
RF plus XWR plus ALUCIN → XWR	III	HHLH	HL	LLL → HHH

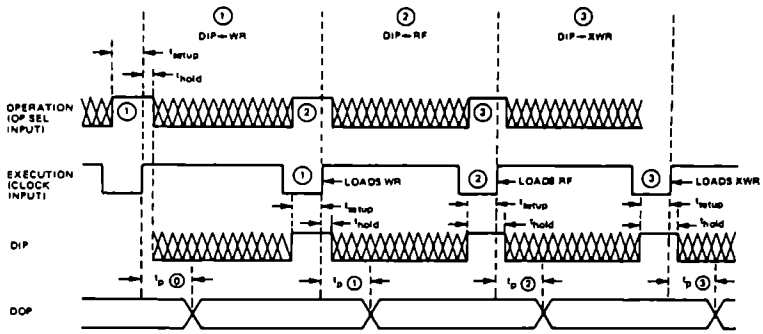
NOTE: When PC priority is low WR → AOP

TABLE 5
RF DESTINATION OPERANDS

OPERATION	OP FORM	OP-FIELD OP3 – OP0	D-FIELD D1 – D0	S-FIELD S2 – S0
DIP → RF	IIIa	HHHH	HL	LLL → HHH
XWR plus ALUCIN → RF	IIg	HHHL	HL	LLL → HHH
RF ALU WR → RF	Ia	LLLL → HHHH	LL	LLL → HHH
RF plus DIP plus ALUCIN → RF	IId	LHHH	HL	LLL → HHH

NOTE: When PC priority is low WR → AOP

A – SBP0400A OPERATION EXECUTION



NOTE: THE SAME CLOCK ① THAT EXECUTES OPERATION ① LOADS OPERATION ② INTO THE '0400A OR.

B – SBP0401A OPERATION EXECUTION

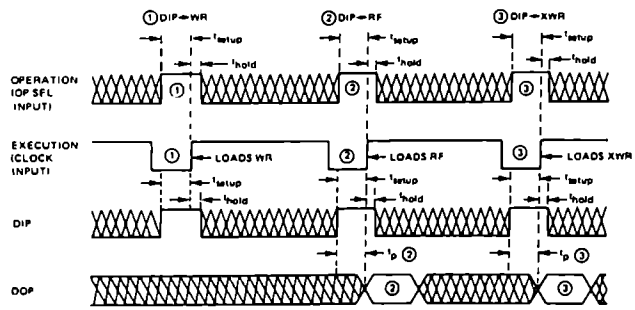


FIGURE 8-TYPICAL OPERATION EXECUTIONS

3.7 PROGRAM COUNTER (PC) – REGISTER FILE SEVEN (RF7)

3.7.1 General Description

RF7 of the register file features the added flexibility of performing as a program counter (PC). Independent of the "present" microinstruction, RF7 may be incremented by a displacement of 1 or 2. Incrementation is accomplished synchronously with the clock and selected, as shown in Table 6, via the multifunction $\overline{\text{PCCIN}}$ and ENINCBY2 inputs as defined by the relative-position control (see Table 3). For cascading purposes, RF7 overflow is provided via the $\overline{\text{PCCOUT}}$ output. Furthermore, RF7 features an independent output bus which allows direct access at the AOP via the ADR multiplexer. When the PC PRIORITY input is taken to a high-logic level, operation select control of the ADR multiplexer is overridden allowing the PC to source the AOP.

TABLE 6
PROGRAM COUNTER INCREMENTATION

RELATIVE POSITION			INPUT		PC IS INCREMENTED ON NEXT CLOCK BY
LSP	IP	MSP	$\overline{\text{PCCIN}}$	ENINCBY2	
YES	NO	NO	H	X	0
			L	L	1
			L	H	2
NO	YES	NO	H	X	0
			L	X	1
NO	NO	YES	H	X	0
			L	X	1

Instruction look-ahead techniques may be employed to boost the system-level efficiency. While the internal operation register of the SBP0400A is directing execution of the "present" microinstruction, the PC may be independently updated to address/fetch data for the "next" microinstruction. In this manner, when the "next" microinstruction becomes the "present" microinstruction as evidenced by its residence in the 0400A OR, steps will have already been taken to fetch an associated data operand.

The SBP0401A, designed for use with the SN54S/74S482 control element, can employ the control memory address register of the 'S482 and other system registers to implement instruction look-ahead or overlap.

3.7.2 PC Configurations

Typical configurations for use of the program counter in an expanded wordlength system are illustrated in Figures 6 and 7. The BMSB/$\overline{\text{PCCOUT}}$ multifunction output may be time multiplexed (see Figure 6) to provide both BMSB and PC overflow (maximum count) status. Under direction of the relative position control (POS1, POS0), the BMSB is available (see Table 3) when POS1 is high, but if POS1 is taken low, $\overline{\text{PCCOUT}}$ is available. After time t_0 the PC contents of the most significant (MSP) will persist until the next L-to-H clock transition. Thus, the BMSB, then $\overline{\text{PCCOUT}}$ data may both be obtained within a single microcycle (1 clock period).

The PC technique shown in Figure 7 may be employed if the required PC wordlength is 4-bits shorter than the processor wordlength. In this situation, the PC's maximum count status is available from the $\overline{\text{PCCOUT}}$ output of the next-to-MSP (IP) package.

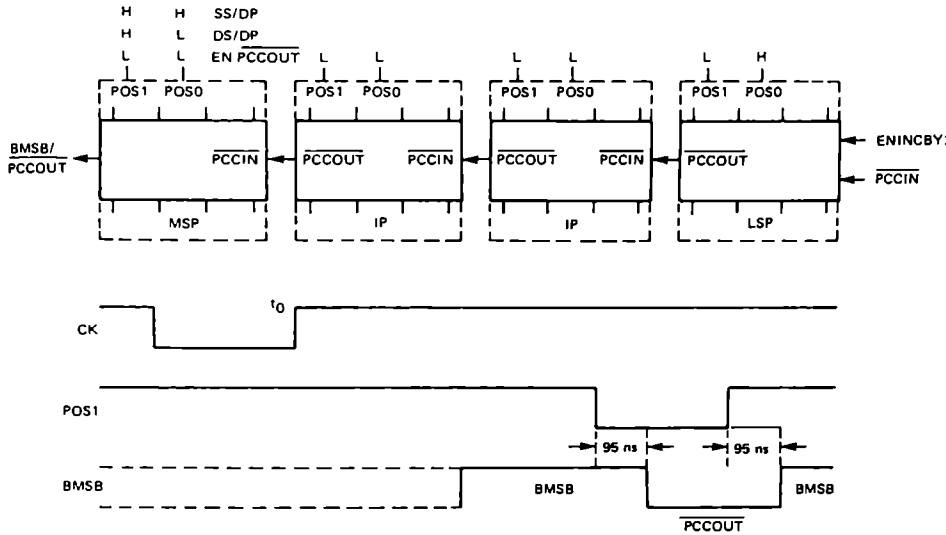
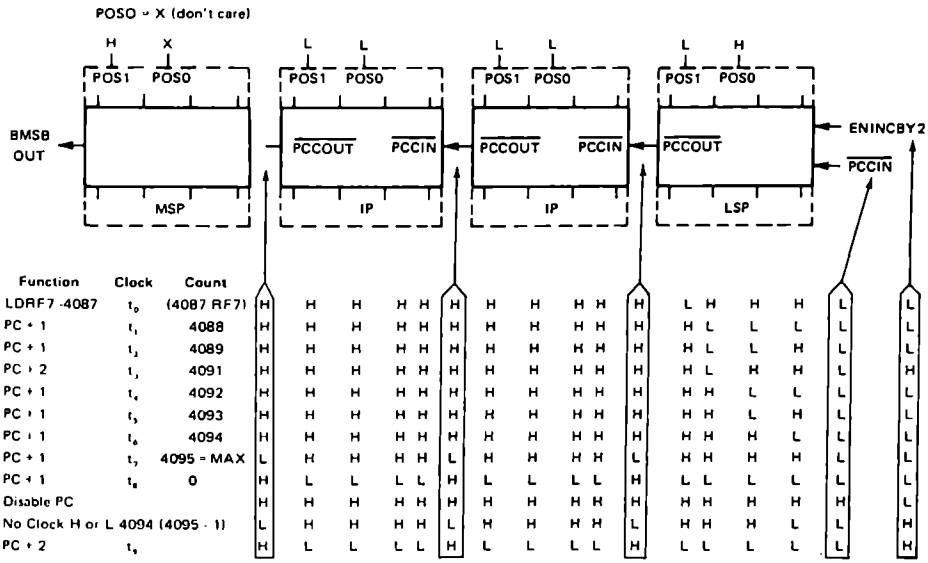


FIGURE 6 – 16-BIT PROGRAM COUNTER



Function	Clock	Count																					
LDRF7 -4087	t_0	(4087 RF7)	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	L	L	L	L	L	L
PC + 1	t_1	4088	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L
PC + 1	t_2	4089	H	H	H	H	H	H	H	H	H	H	H	H	L	L	H	L	L	L	L	L	L
PC + 2	t_3	4091	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	L	L	H	L	L	L
PC + 1	t_4	4092	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
PC + 1	t_5	4093	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	L	L	L	L	L	L
PC + 1	t_6	4094	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L
PC + 1	t_7	4095 = MAX	L	H	H	H	H	L	H	H	H	H	L	H	H	H	H	L	L	L	L	L	L
PC + 1	t_8	0	H	L	L	L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
Disable PC			H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
No Clock H or L 4094 (4095 - 1)			L	H	H	H	H	L	H	H	H	H	L	H	H	H	H	L	L	L	L	H	H
PC + 2	t_9		H	L	L	L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L

FIGURE 7 – 12-BIT PROGRAM COUNTER

3.7.3 PC Count Sequences

PC count sequences initiated at the $\overline{PCCIN}$ and ENINCBY2 inputs of the LSP of an expanded wordlength system are shown in Figure 7. An increment-by-1 command ($\overline{PCCIN}$ = L, ENINCBY2 = L) advances the PC from 4088 to 4089 synchronously with the t_2 clock; an increment-by-2 command ($\overline{PCCIN}$ = L, ENINCBY2 = H) advances the PC from 4089 to 4091 synchronously with the t_3 clock; a PC disable-increment command ($\overline{PCCIN}$ = H) retains the PC at its present count status. When the PC is at maximum count, an increment-by-1 command ($\overline{PCCIN}$ = L, ENINCBY2 = H) conditions the $\overline{PCCOUT}/\overline{PCCIN}$ interpackage carry accommodations such that the PC will increment to zero synchronously with the t_8 clock; when the PC is at maximum-count-minus-1 (N-1), an increment-by-2 command ($\overline{PCCIN}$ = L, ENINCBY2 = H) conditions the $\overline{PCCOUT}/\overline{PCCIN}$ interpackage carry accommodations such that the PC will increment to zero synchronously with the t_9 clock. A maximum count output will be generated at N-1 if the PC is instructed to count by two. This is shown in the supplementary state table of Figure 7.

3.8 ADDRESS-OUT MULTIPLEXER (ADR MUX)

The address-out multiplexer (ADR MUX) is a multiport multiplexer which selects either the WR, XWR, or program counter (PC) for transfer to the address-out port (AOP) via the address-out bus (AOB). When the PC PRIORITY input is logic-level low, ADR MUX transfer of the WR or XWR is selected by the resident operation; when the PC PRIORITY input is logic-level high, resident operation direction of the ADR MUX is overridden allowing the PC to source the AOP.

3.9 A BUS

In addition to 4-bit parallel data transfers, the most significant bit (MSB) of the A bus is available at the multifunction AMSB output if the SBP0400A or SBP0401A is in the most significant position (MSP) as defined by the relative-position control. The AMSB output may be used to monitor the sign-bit of A bus data, or in conjunction with the BMSB and DOP3 (MSP) outputs, to detect an impending ALU overflow condition.

3.10 B BUS

In addition to 4-bit parallel data transfers, the most significant bit (MSB) of the B bus is available at the multifunction BMSB output in the most significant-position (MSP) as defined by the relative-position control. When used with shifts or circulates, this output may be used to extract B-bus data serially from the selected source. The BMSB output may be used to monitor the sign-bit of B bus data, or in conjunction with the AMSB and DOP3 (MSP) outputs, to detect an impending ALU overflow condition.

3.11 WORKING REGISTER (WR)

3.11.1 General Description

The 4-bit working register (WR) is a D-type edge-triggered register which functions as an accumulator for intermediate operands. The WR sources the ALU via the B multiplexer and the address-out-port (AOP) via the ADR multiplexer; the WR is a destination, via the WR multiplexer, for either the data-out bus (DOB) or data-in port (DIP).

3.11.2 WR Source/Destination Operands

Working register source and destination operands are listed in Tables 7 and 8 respectively. When the WR is used as a destination, the source data is recognized only when a low-level condition exists at the clock input. As shown in Figure 5, the source data may change during the low-level clock condition as long as the setup time prior to the low-to-high transition of the clock input is satisfied.

TABLE 7
WORKING REGISTER SOURCE OPERANDS

OPERATION	OP FORM (See 5.3)	OP FIELD OP3 → OP0	D-FIELD D1 → D0	S-FIELD S2 → S0
*WR ALU DIP→ DOP	Ic	LLLL → HHHH	HH	LLL
*WR ALU DIP → WR	Id	LLLL → HHHH	HH	LLH
WR ALU DIP → XWR	If	LLLL → HHHH	HH	HLL
WR ALU RF → RF	Ia	LLLL → HHHH	LL	LLL → HHH
WR ALU RF → WR	Ib	LLLL → HHHH	LH	LLL → HHH
(WR minus DIP minus 1 plus ALUCIN,XWR) LCIR → WR,XWR	IVa	HLLL	HH	LHL
(WR minus DIP minus 1 plus ALUCIN,XWR) RSA → WR,XWR	IVf	LLHL	HH	LHL
(WR minus RF minus 1 plus ALUCIN,XWR) LCIR → WR,XWR	IVc	HLLL	HL	LLL → HHH
(WR minus RF minus 1 plus ALUCIN,XWR) RSA → WR,XWR	IVh	LLHL	HL	LLL → HHH
(WR plus ALUCIN) RSA → WR,XWR	IVe	HLHL	HL	XXX
(WR plus ALUCIN) RSA → WR,XWR	IVe	HLHL	HH	LHL
(WR plus ALUCIN) LCIR → WR	Vd	LLHH	HH	HLH
(WR plus ALUCIN) LCIR → WR	Vd	HLHH	HH	HLH
(WR plus ALUCIN) LSA → WR	Vc	LLHL	HH	HLH
(WR plus ALUCIN) LSL → WR	Vf	HLHL	HH	HLH
(WR plus ALUCIN) RCIR → WR	Vb	LLLH	HH	HLH
(WR plus ALUCIN) RCIR → WR	Vb	HLLH	HH	HLH
(WR plus ALUCIN) RSA → WR	Va	LLLL	HH	HLH
(WR plus ALUCIN) RSL → WR	Ve	HLLL	HH	HLH
(WR plus ALUCIN,XWR) LCIR → (WR,XWR)	VId	HHHH	HH	HLH
(WR plus ALUCIN,HWR) LCIR → (WR,XWR)	VId	LHHH	HH	HLH
(WR plus ALUCIN,XWR) LSA → (WR,XWR)	VIc	LHHL	HH	HLH
(WR plus ALUCIN,XWR) LSL → (WR,XWR)	VIf	HHHL	HH	HLH
(WR plus ALUCIN,XWR) RCIR → (WR,XWR)	VIb	HHLH	HH	HLH
(WR plus ALUCIN,XWR) RCIR → (WR,XWR)	VIb	LHLH	HH	HLH
(WR plus ALUCIN,XWR) RSA → (WR,XWR)	VIa	LHLL	HH	HLH
(WR plus ALUCIN,XWR) RSL → (WR,XWR)	VIe	HHLL	HH	HLH
WR plus DIP plus ALUCIN → DOP	IIi	LHHH	HH	LHL
WR plus DIP plus ALUCIN → XWR	IIh	LLHH	HH	LHL
(WR plus DIP plus ALUCIN) LCIR → WR,XWR	IVb	HLLH	HH	LHL
(WR plus DIP plus ALUCIN) RSA → WR,XWR	IVg	HLHH	HH	LHL
WR plus RF plus ALUCIN → XWR	IIa	LLHH	HL	LLL → HHH
(WR plus RF plus ALUCIN) LCIR → WR,XWR	IVd	HLLH	HL	LLL → HHH
(WR plus RF plus ALUCIN) RSA → WR,XWR	IVi	HLHH	HL	LLL → HHH

NOTE: When PC priority is low WR → AOP
*XWR → AOP

TABLE 8
WORKING REGISTER DESTINATION OPERANDS

OPERATION	OP FORM (See 5.3)	OP-FIELD OP3 - OP0	D-FIELD D1 - D0	S-FIELD S2 - S0
WR ALU RF - WR	Ib	LLLL - HHHH	LH	LLL - HHH
(WR minus DIP minus 1 plus ALUCIN,XWR) LCIR - WR,XWR	IVa	HLLL	HH	LHL
(WR minus DIP minus 1 plus ALUCIN,XWR) RSA - WR,XWR	IVd	LLHL	HH	LHL
(WR minus RF minus 1 plus ALUCIN,XWR) LCIR - WR,XWR	IVc	HLLL	HL	LLL - HHH
(WR minus RF minus 1 plus ALUCIN,XWR) RSA - WR,XWR	IVh	LLHL	HL	LLL - HHH
(WR plus ALUCIN) RSA - WR,XWR	IVe	HLHL	HL	XXX
(WR plus ALUCIN) RSA - WR,XWR	IVe	HLHL	HH	LHL
(WR plus ALUCIN) LCIR - WR	Vd	LLHH	HH	HLH
(WR plus ALUCIN) LCIR - WR	Vd	HLHH	HH	HLH
(WR plus ALUCIN) LSA - WR	Vc	LLHL	HH	HLH
(WR plus ALUCIN) LSL - WR	VI	HLHL	HH	HLH
(WR plus ALUCIN) RCIR - WR	Vb	LLLH	HH	HLH
(WR plus ALUCIN) RCIR - WR	Vb	HLLH	HH	HLH
(WR plus ALUCIN) RSA - WR	Va	LLLL	HH	HLH
(WR plus ALUCIN) RSL - WR	Ve	HLLL	HH	HLH
(WR plus ALUCIN, XWR) LCIR - (WR, XWR)	VId	HHHH	HH	HLH
(WR plus ALUCIN, XWR) LCIR - (WR, XWR)	VId	LHHH	HH	HLH
(WR plus ALUCIN, XWR) LSA - (WR, XWR)	VIc	LHHL	HH	HLH
(WR plus ALUCIN, XWR) LSL - (WR, XWR)	VIf	HHHL	HH	HLH
(WR plus ALUCIN, XWR) RCIR - (WR, XWR)	VIb	HHLH	HH	HLH
(WR plus ALUCIN, XWR) RCIR - (WR, XWR)	VIb	LHLH	HH	HLH
(WR plus ALUCIN, XWR) RSA - (WR,XWR)	VIa	LHLL	HH	HLH
(WR plus ALUCIN, XWR) RSL - (WR, XWR)	VIe	HHLL	HH	HLH
(WR plus DIP plus ALUCIN) LCIR - WR, XWR	IVb	HLLH	HH	LHL
(WR plus DIP plus ALUCIN) RSA - WR, XWR	IVg	HLHH	HH	LHL
(WR plus RF plus ALUCIN) LCIR - WR, XWR	IVd	HLLH	HL	LLL - HHH
(WR plus RF plus ALUCIN) RSA - WR, XWR	IVi	HLHH	HL	LLL - HHH

NOTE: When PC PRIORITY is low WR - AOP

* XWR - AOP

3.11.3 WR Sourcing of ADR MUX

The resident operation directs the WR to source the AOP via the ADR multiplexer during 427 of the 459 possible unique operations. In the cases of operation form-type Ic and Id (see Table 27) which represent the remaining 32 of the 459 possible unique operations, the resident operation directs the XWR to source the AOP via the ADR. When the PC PRIORITY input is at a high-logic level, resident operation direction of the ADR multiplexer is overridden allowing the PC to source the AOP.

3.12 EXTENDED WORKING REGISTER (XWR)

3.12.1 XWR General Description

The 4-bit extended working register (XWR) is a D-type edge-triggered register which functions as 1) an accumulator during address derivations and 2) a WR extension during operations where double-length operands are present/

accumulated (iterative non-restoring divide, double-precision shifts/circulates, iterative multiply, etc.). The XWR sources 1) the ALU via the B multiplexer, 2) the AOP via the ADR multiplexer, or 3) itself shifted right or left via the XWR multiplexer. The XWR is a destination via the XWR multiplexer for either the DOB or the XWR, itself, shifted right or left.

3.12.2 XWR Source/Destination Operands

Extended working register source and destination operands are listed in Tables 9 and 10 respectively.

TABLE 9
EXTENDED WORKING REGISTER SOURCE OPERANDS

OPERATION	OP FORM (See 5.3)	OP-FIELD OP3 – OP0	D-FIELD D1 – D0	S-FIELD S2 – S0
XWR ALU DIP → DOP	Ih	LLLL – HHHH	HH	HHH
XWR ALU DIP → WR	Ie	LLLL – HHHH	HH	LHH
XWR ALU DIP → XWR	Ig	LLLL – HHHH	HH	HHL
XWR plus ALUCIN → DOP	Ili	HHHL	HH	LHL
XWR plus ALUCIN → RF	Ilj	HHHL	HL	LLL – HHH
XWR plus DIP plus ALUCIN → WR	Ilk	HHLL	HH	LHL
XWR plus DIP plus ALUCIN → XWR	Ilf	HHLH	HH	LHL
XWR plus RF plus ALUCIN → WR	Ile	HHLL	HL	LLL – HHH

NOTE When PC PRIORITY is low WR → AOP

TABLE 10
WORKING REGISTER DESTINATION OPERANDS

OPERATION	OP FORM (See 5.3)	OP FIELD OP3 – OP0	D-FIELD D1 – D0	S-FIELD S2 – S0
DIP ALU XWR → XWR	Ig	LLLL – HHHH	HH	HHL
WR ALU DIP → XWR	If	LLLL – HHHH	HH	HLL
(WR minus DIP minus 1 plus ALUCIN, XWR) LCIR → WR, XWR	IVa	HLLL	HH	LHL
(WR minus DIP minus 1 plus ALUCIN, XWR) RSA → WR, XWR	IVf	LLHL	HH	LHL
(WR minus RF minus 1 plus ALUCIN, XWR) LCIR → WR, XWR	IVc	HLLL	HL	LLL – HHH
(WR minus RF minus 1 plus ALUCIN, XWR) RSA → WR, XWR	IVh	LLHL	HL	LLL – HHH
(WR plus ALUCIN) RSA → WR, XWR	IVe	HLHL	HL	XXX
(WR plus ALUCIN) RSA → WR, XWR	IVe	HLHL	HH	LHL
(WR plus ALUCIN, XWR) LCIR → (WR, XWR)	VId	HHHH	HH	HLH
(WR plus ALUCIN, XWR) LCIR → (WR, XWR)	VId	LHHH	HH	HLH
(WR plus ALUCIN, XWR) LSA → (WR, XWR)	VIc	LHHL	HH	HLH
(WR plus ALUCIN, XWR) LSL → (WR, XWR)	VIf	HHHL	HH	HLH
(WR plus ALUCIN, XWR) RCIR → (WR, XWR)	VIb	HHLH	HH	HLH
(WR plus ALUCIN, XWR) RCIR → (WR, XWR)	VIb	LHLH	HH	HLH
(WR plus ALUCIN, XWR) RSA → (WR, XWR)	VIa	LHLL	HH	HLH
(WR plus ALUCIN, XWR) RSL → (WR, XWR)	VIe	HHLL	HH	HLH
WR plus DIP plus ALUCIN → XWR	IIh	LLHH	HH	LHL
(WR plus DIP plus ALUCIN) LCIR → WR, XWR	IVb	HLLH	HH	LHL
(WR plus DIP plus ALUCIN) RSA → WR, XWR	IVg	HLHH	HH	LHL
WR plus RF plus ALUCIN → XWR	IIa	LLHH	HL	LLL → HHH
(WR plus RF plus ALUCIN) LCIR → WR, XWR	IVd	HLLH	HL	LLL → HHH
(WR plus RF plus ALUCIN) RSA → WR, XWR	IVi	HLHH	HL	LLL → HHH
DIP plus XWR plus ALUCIN → XWR	IIk	HHLH	HH	LHL
DIP → XWR	IIIe	LLLH	HH	LHL

NOTE: When PC PRIORITY is low WR → AOP

When the XWR is used as a destination, the source data is recognized only when a low-level condition exists at the clock input. As shown in Figure 5, the source data can change during the low-level clock condition as long as the setup time prior to the low-to-high transition of the clock input is satisfied.

3.12.3 XWR Sourcing of ADR MUX

Operation form-type Ic and Id (see Table 27) represent 32 of the 459 possible unique operations. During these operations the resident operation directs the XWR to source the AOP via the ADR multiplexer. During the remaining 427 of the 459 possible operations, the resident operation directs the WR to source the AOP via the ADR multiplexer. When the PC PRIORITY input is at a high-logic level, resident operation direction of the ADR multiplexer is overridden allowing the PC to source the AOP.

3.13 DATA-OUT MULTIPLEXER (DO MUX)

3.13.1 DO MUX General Description

The data-out multiplexer (DO MUX) is a multi-port, special purpose multiplexer which provides scaled shifting of the ALU output, and direct transfer of the A bus to the data-out bus, bypassing the ALU. The output port of the DO MUX provides, in accordance with Table 11, ALU output data not shifted, ALU output data shifted right one bit position, ALU output data shifted left one bit position, and A bus data not shifted. Control for the DO MUX is provided by the resident operation in conjunction with the relative position control.

TABLE 11
DO MUX TRANSFERS

	OPERATION TYPE	DO MUX OUTPUT			
		3	2	1	0
INTERMEDIATE AND LEAST SIGNIFICANT POSITIONS	RIGHT SHIFT ARITHMETIC	WRLFT	ALU3	ALU2	ALU1
	RIGHT SHIFT LOGICAL	WRLFT	ALU3	ALU2	ALU1
	RIGHT CIRCULATE	WRLFT	ALU3	ALU2	ALU1
	ALU OUT BUS → DATA-OUT BUS	ALU3	ALU2	ALU1	ALU0
	A BUS → DATA-OUT BUS	ABUS3	ABUS2	ABUS1	ABUS0
	LEFT SHIFT ARITHMETIC	ALU2	ALU1	ALU0	WRRT
	LEFT SHIFT LOGICAL	ALU2	ALU1	ALU0	WRRT
	LEFT CIRCULATE	ALU2	ALU1	ALU0	WRRT
MOST SIGNIFICANT POSITION (MSP)	RIGHT SHIFT ARITHMETIC	WR3	ALU3	ALU2	ALU1
	RIGHT SHIFT LOGICAL	WRLFT	ALU3	ALU2	ALU1
	RIGHT CIRCULATE	WRLFT	ALU3	ALU2	ALU1
	ALU OUT BUS → DATA-OUT BUS	ALU3	ALU2	ALU1	ALU0
	A BUS → DATA-OUT BUS	ABUS3	ABUS2	ABUS1	ABUS0
	LEFT SHIFT ARITHMETIC	ALU2	ALU1	ALU0	WRRT
	LEFT SHIFT LOGICAL	ALU2	ALU1	ALU0	WRRT
	LEFT CIRCULATE	ALU2	ALU1	ALU0	WRRT

3.13.2 DO MUX Shift Accommodations

Special bidirectional shift accommodations are provided to or from each end of the DO MUX to facilitate interpackage data shifts in expanded word length systems. The direction of these shift accommodations is selected by the resident operation. Bit 3 (MSB) of the DO MUX for each processor element receives interpackage right shift data and transmits interpackage left shift data via the bidirectional shift accommodation $\overline{\text{WRLFT}}$; bit 0 (LSB) receives interpackage left shift data and transmits interpackage right shift data via the bidirectional shift accommodation $\overline{\text{WRRT}}$. Both $\overline{\text{WRLFT}}$ and $\overline{\text{WRRT}}$, low-active signals at the package terminals, become WRLFT and WRRT, respectively, high-active signals within the processor element.

3.14 DATA-OUT I-MULTIPLEXER (DO IMUX)

The data-out I-multiplexer (DO IMUX) is a special purpose multiplexer which outputs, in accordance with Table 12, appropriate left-shift data via the bidirectional shift accommodation $\overline{\text{WRLFT}}$. Control for the DO IMUX is provided by the resident operation in conjunction with the relative position control.

TABLE 12
DO IMUX TRANSFERS TO $\overline{\text{WRLFT}}$

	OPERATION TYPE	DO IMUX OUTPUT TO $\overline{\text{WRLFT}}$
INTERMEDIATE (IP) AND LEAST SIGNIFICANT POSITIONS (LSP)	LEFT SHIFT ARITHMETIC LEFT SHIFT LOGICAL LEFT CIRCULATE	$\overline{\text{ALU3}}$ $\overline{\text{ALU3}}$ $\overline{\text{ALU3}}$
MOST SIGNIFICANT POSITION (MSP) SINGLE-PRECISION (SP) SHIFTS/CIRCULATES	LEFT SHIFT ARITHMETIC LEFT SHIFT LOGICAL LEFT CIRCULATE	HIGH HIGH $\overline{\text{ALU3}}$
MOST SIGNIFICANT POSITION (MSP) SINGLE-SIGNED/DOUBLE-PRECISION (SS/DP) SHIFTS/CIRCULATES	LEFT SHIFT ARITHMETIC LEFT SHIFT LOGICAL LEFT CIRCULATE	$\overline{\text{XWR3}}$ $\overline{\text{XWR3}}$ $\overline{\text{XWR3}}$
MOST SIGNIFICANT POSITION (MSP) DOUBLE-SIGNED/DOUBLE-PRECISION (DS/DP) SHIFTS/CIRCULATES	LEFT SHIFT ARITHMETIC LEFT SHIFT LOGICAL LEFT CIRCULATE	$\overline{\text{XWR2}}$ $\overline{\text{XWR3}}$ $\overline{\text{XWR3}}$

3.15 DATA-OUT J-MULTIPLEXER (DO JMUX)

The data-out J-multiplexer (DO JMUX) is a special purpose multiplexer which outputs, as per Table 13, appropriate right shift data via the bidirectional shift accommodation $\overline{\text{WRRT}}$. Control for the DO JMUX is provided by the resident operation in conjunction with the relative position control.

TABLE 13
DO JMUX TRANSFERS TO $\overline{\text{WRRT}}$

	OPERATION TYPE	DO JMUX OUTPUT TO $\overline{\text{WRRT}}$
MOST-SIGNIFICANT (MSP) OR INTER-MEDIATE (IP) POSITIONS	RIGHT SHIFT ARITHMETIC RIGHT SHIFT LOGICAL RIGHT CIRCULATE	$\overline{\text{ALU0}}$ $\overline{\text{ALU0}}$ $\overline{\text{ALU0}}$
LEAST-SIGNIFICANT POSITION (LSP) SINGLE-PRECISION (SP) SHIFTS/ CIRCULATES	RIGHT SHIFT ARITHMETIC RIGHT SHIFT LOGICAL RIGHT CIRCULATE	HIGH HIGH $\overline{\text{ALU0}}$
LEAST-SIGNIFICANT POSITION (LSP) DOUBLE-PRECISION (DP) SHIFTS/ CIRCULATES	RIGHT SHIFT ARITHMETIC RIGHT SHIFT LOGICAL RIGHT CIRCULATE	HIGH HIGH $\overline{\text{XWR0}}$

3.16 EXTENDED WORKING REGISTER MULTIPLEXER (XWR MUX)

3.16.1 XWR MUX General Description

The extended working register multiplexer (XWR MUX) is a multi-port, special purpose multiplexer which provides scaled shifting of the XWR outputs and direct transfer of the data-out bus to the XWR input. The output port of the XWR MUX provides, in accordance with Table 14, XWR output data shifted left one bit position, XWR output data shifted right one bit position, and data-out bus data not shifted. The XWR MUX also sources the XWR MSB/LSB output. Under control of the relative position inputs, in the MSP the XWR MUX MSB (Bit 3) is available at the XWR MSB output and in the LSP the XWR MUX LSB (Bit 0) is available at the XWR LSB output. Control for the XWR MUX is provided by the resident operation in conjunction with the relative position control.

3.16.2 XWR MUX Shift Accommodations

Special bidirectional shift accommodations are provided to or from each end of the XWR MUX to facilitate interpackage data shifts when the processor element is used in expanded word length systems. Bit 3 (MSB) or bit 2 of the XWR MUX is selected by the resident operation in conjunction with the relative position control to receive double-precision interpackage right shift data or transmit double-precision interpackage left shift data via the bidirectional shift accommodation $\overline{\text{XWRLFT}}$; bit 0 (LSB) receives double-precision interpackage left shift data and

TABLE 14
XWR MUX TRANSFERS

	OPERATION TYPE (DOUBLE-PRECISION)	XWR MUX OUTPUT			
		3	2	1	0
MOST-SIGNIFICANT POSITION (MSP)	RIGHT SHIFT ARITHMETIC SINGLE-SIGNED	XWRLFT	XWR3	XWR2	XWR1
	RIGHT SHIFT ARITHMETIC DOUBLE-SIGNED	XWR3	XWRLFT	XWR2	XWR1
	RIGHT SHIFT LOGICAL	XWRLFT	XWR3	XWR2	XWR1
	RIGHT CIRCULATE	XWRLFT	XWR3	XWR2	XWR1
	DATA-OUT-BUS -- XWR	DOB3	DOB2	DOB1	DOB0
	LEFT SHIFT ARITHMETIC SINGLE-SIGNED	XWR2	XWR1	XWR0	XWRRT
	LEFT SHIFT ARITHMETIC DOUBLE-SIGNED	ALU2	XWR1	XWR0	XWRRT
	LEFT SHIFT LOGICAL	XWR2	XWR1	XWR0	XWRRT
	LEFT CIRCULATE	XWR2	XWR1	XWR0	XWRRT
LEAST-SIGNIFICANT OR INTERMEDIATE POSITION (IP)	RIGHT SHIFT ARITHMETIC SINGLE-SIGNED	XWRLFT	XWR3	XWR2	XWR1
	RIGHT SHIFT ARITHMETIC DOUBLE-SIGNED	XWRLFT	XWR3	XWR2	XWR1
	RIGHT SHIFT LOGICAL	XWRLFT	XWR3	XWR2	XWR1
	RIGHT CIRCULATE	XWRLFT	XWR3	XWR2	XWR1
	DATA-OUT-BUS -- XWR	DOB3	DOB2	DOB1	DOB0
	LEFT SHIFT ARITHMETIC SINGLE-SIGNED	XWR2	XWR1	XWR0	XWRRT
	LEFT SHIFT ARITHMETIC DOUBLE-SIGNED	XWR2	XWR1	XWR0	XWRRT
	LEFT SHIFT LOGICAL	XWR2	XWR1	XWR0	XWRRT
	LEFT CIRCULATE	XWR2	XWR1	XWR0	XWRRT

transmits interpackage right shift data via the bidirectional shift accommodation $\overline{\text{XWRRT}}$. Both $\overline{\text{XWRLFT}}$ and $\overline{\text{XWRRT}}$, low-active signals at the package terminals, become XWRLFT and XWRRT, respectively, high-active signals within the processor element.

3.17 EXTENDED WORKING REGISTER K-MULTIPLEXER (XWR KMUX)

The extended working register K-multiplexer (XWR KMUX) is a special purpose multiplexer which outputs, in accordance with Table 15, appropriate double-precision left-shift data via the bidirectional shift accommodation $\overline{\text{XWRLFT}}$. Control for the XWR KMUX is provided by the resident operation in conjunction with the relative position control.

TABLE 15
XWR KMUX TRANSFERS TO $\overline{\text{XWRLFT}}$

	OPERATION TYPE (DOUBLE-PRECISION)	XWR KMUX OUTPUT TO $\overline{\text{XWRLFT}}$
LEAST-SIGNIFICANT OR INTERMEDIATE POSITIONS (IP)	LEFT SHIFT ARITHMETIC SINGLE-SIGNED	$\overline{\text{XWR3}}$
	LEFT SHIFT ARITHMETIC DOUBLE-SIGNED	$\overline{\text{XWR3}}$
	LEFT SHIFT LOGICAL	$\overline{\text{XWR3}}$
	LEFT CIRCULATE	$\overline{\text{XWR3}}$
MOST-SIGNIFICANT POSITION	LEFT SHIFT ARITHMETIC SINGLE-SIGNED	HIGH
	LEFT SHIFT ARITHMETIC DOUBLE-SIGNED	HIGH
	LEFT SHIFT LOGICAL	HIGH
	LEFT CIRCULATE	$\overline{\text{ALU3}}$

3.18 EXTENDED WORKING REGISTER L MULTIPLEXER (XWR LMUX)

The extended working register L multiplexer (XWR LMUX) is a special purpose multiplexer which outputs, in accordance with Table 16, appropriate double-precision right shift data via the bidirectional shift accommodation $\overline{XWRRT}$. Control for the XWR LMUX is provided by the resident operation in conjunction with the relative position control.

TABLE 16
XWR LMUX TRANSFERS TO $\overline{XWRRT}$

	OPERATION TYPE (DOUBLE-PRECISION)	XWR LMUX OUTPUT TO $\overline{XWRRT}$
MOST-SIGNIFICANT (MSP) OR INTERMEDIATE POSITIONS (IP)	RIGHT SHIFT ARITHMETIC SINGLE-SIGNED	$\overline{XWR0}$
	RIGHT SHIFT ARITHMETIC DOUBLE-SIGNED	$\overline{XWR0}$
	RIGHT SHIFT LOGICAL	$\overline{XWR0}$
	RIGHT CIRCULATE	$\overline{XWR0}$
LEAST-SIGNIFICANT POSITION (LSP)	RIGHT SHIFT ARITHMETIC SINGLE-SIGNED	$\overline{ALU0}$
	RIGHT SHIFT ARITHMETIC DOUBLE-SIGNED	$\overline{ALU0}$
	RIGHT SHIFT LOGICAL	$\overline{ALU0}$
	RIGHT CIRCULATE	$\overline{ALU0}$

3.19 WORKING REGISTER MULTIPLEXER (WR MUX)

The working register multiplexer (WR MUX) is a multi-port multiplexer which, under control of the resident operation, selects either data-in port data or data-out bus data for direct transfer to the WR.

4. SHIFT/CIRCULATE OPERATIONS

The SBP0400A and the SBP0401A uses the DO MUX in conjunction with the DO IMUX and DO JMUX to accomplish single-bit WR shift/circulate operations; the XWR MUX in conjunction with the XWR KMUX and XWR LMUX to accomplish single-bit XWR shift/circulate operations. While single-precision shift/circulate operations involve the WR only, double-precision shift/circulate operations involve the WR in conjunction with the XWR. The standard operation set does not include single-precision XWR shift/circulate operations.

4.1 WR SINGLE-PRECISION SHIFTS/CIRCULATES

WR single-precision shift/circulate operations are directed by the resident operation with expanded wordlength "end" conditions handled by the relative position controls. These single-precision operations may best be represented by the generalized symbol:

(WR plus ALUCIN) SHIFTED/CIRCULATED → WR

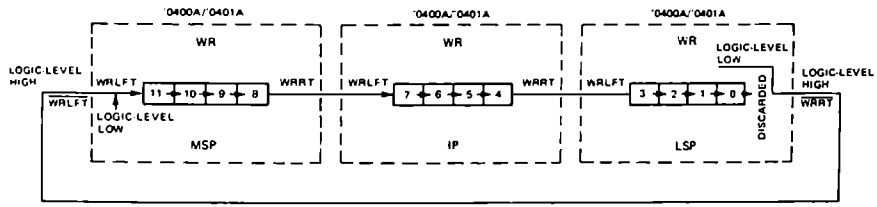
Within a single microcycle (1 clock period), each of six possible WR single-precision shift/circulate operations is capable of 1) asynchronously summing the WR with the ALUCIN input, then 2) asynchronously shifting/circulating the sum one bit position to the right/left, and finally 3) synchronously storing the shifted/circulated result back into the WR. The six WR single-precision shift/circulate possibilities, with data flow paths for expanded wordlengths, are listed in Table 17.

TABLE 17
WR SINGLE-PRECISION SHIFTS/CIRCULATES

SHIFT/CIRCULATE OPERATION	SHIFT/CIRCULATE FUNCTION	EXPANDED WORDLENGTH DATA FLOW PATHS	OP-FORM (See 5.3)	OP-FIELD OP3 → OP0	D-FIELD D1 → D0	B-FIELD B2 → B0
(WR plus ALUCIN) RSL → WR	RIGHT SHIFT LOGICAL (RSL)	Figure 8	Ve	HLLL	HH	HLH
(WR plus ALUCIN) LSL → WR	LEFT SHIFT LOGICAL (LCL)	Figure 9	Vf	HLHL	HH	HLH
(WR plus ALUCIN) RSA → WR	RIGHT SHIFT ARITHMETIC (RSA)	Figure 10	Va	LLLL	HH	HLH
(WR plus ALUCIN) LSA → WR	LEFT SHIFT ARITHMETIC (LSA)	Figure 11	Vc	LLHL	HH	HLH
(WR plus ALUCIN) RCIR → WR	RIGHT CIRCULATE (RCIR)	Figure 12	Vb	LLLH	HH	HLH
(WR plus ALUCIN) LCIR → WR	LEFT CIRCULATE (LCIR)	Figure 13	Vd	LLHH	HH	HLH

4.1.1 (WR Plus ALUCIN) RSL → WR

The WR single-precision logical right-shift operation, shown in Figure 8, displaces the entire contents of the WR one bit position to the right. In an expanded wordlength system, a logic-level low is automatically right-shifted into the WR's most-significant-bit (MSB) of the most-significant-package (MSP) as the WR's contents are displaced to the right. This logic-level low, sourced by the least-significant-package (LSP), exits the LSP via the bidirectional shift accommodation $\overline{\text{WRRT}}$ and enters the MSP via the bidirectional shift accommodation $\overline{\text{WRLFT}}$. During each WR RSL operation, the WR's displaced LSB of the LSP is discarded.

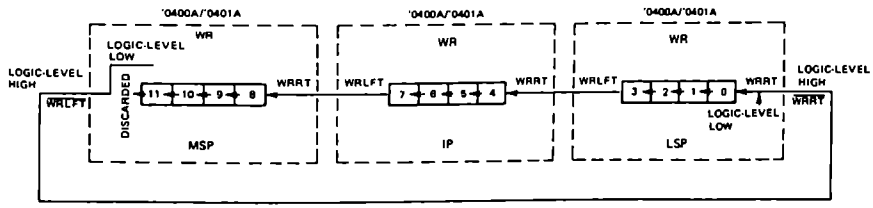


NOTE: WRRT, WRLFT, ARE HIGH-ACTIVE INTRA-PACKAGE AND LOW-ACTIVE (INVERSE POLARITY) INTER-PACKAGE

FIGURE 8 – RIGHT SHIFT LOGICAL – SINGLE PRECISION (RSL – SP)

4.1.2 (WR Plus ALUCIN) LSL → WR

The WR single-precision logical left-shift operation, shown in Figure 9, displaces the entire contents of the WR one bit position to the left. In an expanded wordlength system, a logic-level low is automatically left-shifted into the WR's LSB of the LSP as the WR's contents are displaced to the left. This logic-level low, sourced by the MSP, exits the MSP via the bidirectional shift accommodation $\overline{\text{WRLFT}}$ and enters the LSP via the bidirectional shift accommodation $\overline{\text{WRRT}}$. During each WR LSL operation, the WR's displaced MSB of the MSP is discarded.

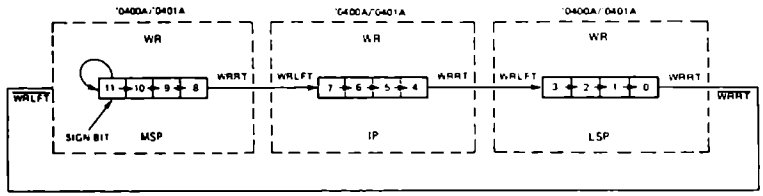


NOTE: WRRT, WRLFT, ARE HIGH-ACTIVE INTRA-PACKAGE AND LOW-ACTIVE (INVERSE POLARITY) INTER-PACKAGE

FIGURE 9 – LEFT SHIFT LOGICAL – SINGLE PRECISION (LSL – SP)

4.1.3 (WR Plus ALUCIN) RSA → WR

The WR single-precision arithmetic right-shift operation, shown in Figure 10, displaces the entire contents of the WR one bit position to the right. The MSB of the MSP is designated as a sign-bit. As the entire contents of the WR is displaced to the right, the sign-bit does *not* change. Rather the sign-bit is duplicated to the right. The displaced LSB of the LSP exits the LSP via the bidirectional shift accommodation $\overline{\text{WRRT}}$.

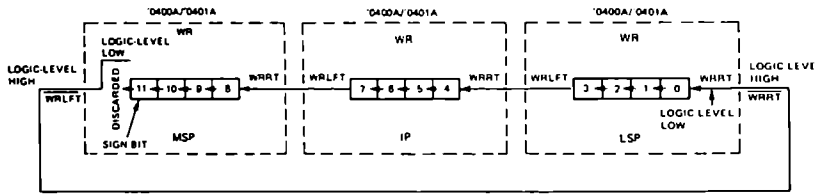


NOTE: WRRT, WRLFT, ARE HIGH-ACTIVE (INTRA-PACKAGE) AND LOW-ACTIVE (INVERSE POLARITY) (INTER-PACKAGE)

FIGURE 10 – RIGHT SHIFT ARITHMETIC – SINGLE PRECISION (RSA – SP)

4.1.4 (WR Plus ALUCIN) LSA → WR

The WR single-precision arithmetic left-shift operation, shown in Figure 11, is functionally identical to the WR single-precision logical left-shift operation. The WR's MSB of the MSP, although designated as a sign-bit, is discarded as the entire contents of the WR is displaced one bit position to the left. As each WR LSA operation is performed, the BMSB output (WR sign bit) may be compared to the MSB of the MSP's DOP (data displacing into WR sign bit) to detect an impending change in WR sign-bit polarity.

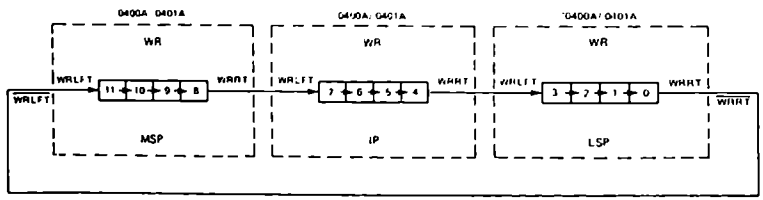


NOTE: WRRT, WRLFT, ARE HIGH-ACTIVE (INTRA-PACKAGE) AND LOW-ACTIVE (INVERSE POLARITY) (INTER-PACKAGE)

FIGURE 11 – LEFT SHIFT ARITHMETIC – SINGLE PRECISION (LSA – SP)

4.1.5 (WR Plus ALUCIN) RCIR → WR

The WR single-precision right-circulate operation, shown in Figure 12, displaces the entire contents of the WR one bit position to the right. The displaced LSB of the LSP replaces the displaced MSB of the MSP. The displaced LSB of the LSP exits the LSP via the bidirectional shift accommodation $\overline{\text{WRRT}}$ and enters the MSP via the bidirectional shift accommodation $\overline{\text{WRLFT}}$.

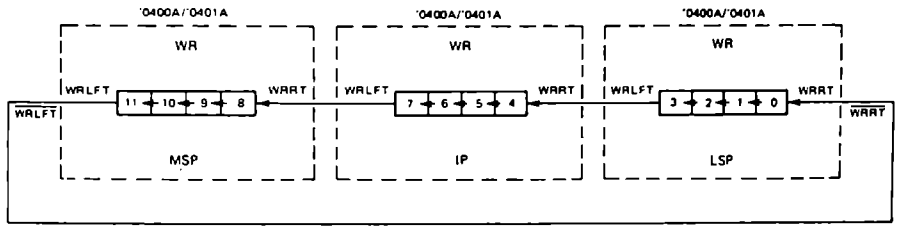


NOTE: WRRT, WRLFT, ARE HIGH-ACTIVE (INTRA-PACKAGE) AND LOW-ACTIVE (INVERSE POLARITY) (INTER-PACKAGE)

FIGURE 12 – RIGHT CIRCULATE – SINGLE PRECISION (RCIR – SP)

4.1.6 (WR Plus ALUCIN) LCIR → WR

The WR single-precision left-circulate operation, shown in Figure 13, displaces the entire contents of the WR one bit position to the left. The displaced MSB of the MSP replaces the displaced LSB of the LSP. The displaced MSB of the MSP exits the MSP via the bidirectional shift accommodation $\overline{\text{WRLFT}}$ and enters the LSP via its bidirectional shift accommodation $\overline{\text{WRRT}}$.



NOTE: WRRT, WRLFT, ARE HIGH-ACTIVE INTRA-PACKAGE AND LOW-ACTIVE (INVERSE POLARITY) INTER-PACKAGE.

FIGURE 13 – LEFT CIRCULATE – SINGLE PRECISION (LCIR – SP)

4.2 WR,XWR DOUBLE-PRECISION SHIFTS/CIRCULATES

WR,XWR double-precision shift/circulate operations are directed by the resident operation with expanded wordlength "end" conditions handled by the relative position controls. The double-precision shift/circulate operations may best be represented by the generalized symbol:

(WR plus ALUCIN, XWR) SHIFTED/CIRCULATED → WR,XWR

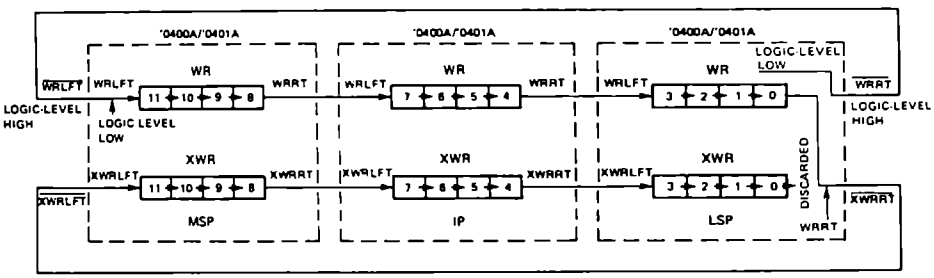
Within a single microcycle, each of eight possible WR,XWR double-precision shift/circulate operations is capable of 1) asynchronously summing the WR with the ALUCIN input, then 2) asynchronously double-precision shifting/circulating the sum with the WR and XWR considered as one double-length register, and finally 3) synchronously storing the shifted/circulated result into the double-length register formed by WR in conjunction with the XWR. The eight WR,XWR double-precision shift/circulate possibilities, with data flow paths for expanded wordlengths, are listed in Table 18.

TABLE 18
WR, XWR DOUBLE-PRECISION SHIFTS/CIRCULATES

SHIFT/CIRCULATE OPERATION	SHIFT/CIRCULATE FUNCTION	EXPANDED WORDLENGTH DATA FLOW PATHS	OP-FORM (See 8.3)	OP-FIELD OP3 – OP0	D-FIELD D1 – D0	S-FIELD S2 – S0
(WR plus ALUCIN, XWR) RSL → WR, XWR	RIGHT-SHIFT-LOGICAL (RSL)	Figure 14	VIa	HHLL	HH	HLH
(WR plus ALUCIN, XWR) LSL → WR, XWR	LEFT SHIFT-LOGICAL (LSL)	Figure 15	VIf	HHHL	HH	HLH
(WR plus ALUCIN, XWR) RSA → WR, XWR	RIGHT-SHIFT-ARITHMETIC (RSA)	Figure 16, 17	VIa	LHLL	HH	HLH
(WR plus ALUCIN, XWR) LSA → WR, XWR	LEFT-SHIFT-ARITHMETIC (LSA)	Figure 18, 19	VIc	LHHL	HH	HLH
(WR plus ALUCIN, XWR) RCIR → WR, XWR	RIGHT-CIRCULATE (RCIR)	Figure 20	VIb	LHLH	HH	HLH
(WR plus ALUCIN, XWR) LCIR → WR, XWR	LEFT-CIRCULATE (LCIR)	Figure 21	VIJ	LHHH	HH	HLH

4.2.1 (WR Plus ALUCIN, XWR) RSL → WR,XWR

The WR,XWR double-precision logical right-shift operation, shown in Figure 14, displaces the entire contents of the double-length register, formed by the WR in conjunction with the XWR, one bit position to the right. In an expanded wordlength system, the WR's displaced LSB of the LSP exits the LSP via the bidirectional shift accommodation $\overline{\text{XWRRT}}$ and enters the XWR's MSB of the MSP via the bidirectional shift accommodation $\overline{\text{XWRLFT}}$. A logic-level low is automatically right-shifted into the WR's MSB of the MSP. This logic-level low, sourced by the LSP, exits the LSP via the bidirectional shift accommodation $\overline{\text{WRRT}}$ and enters the MSP via the bidirectional shift accommodation $\overline{\text{WRLFT}}$. During each WR,XWR RSL operation, the XWR's displaced LSB of the LSP is discarded.

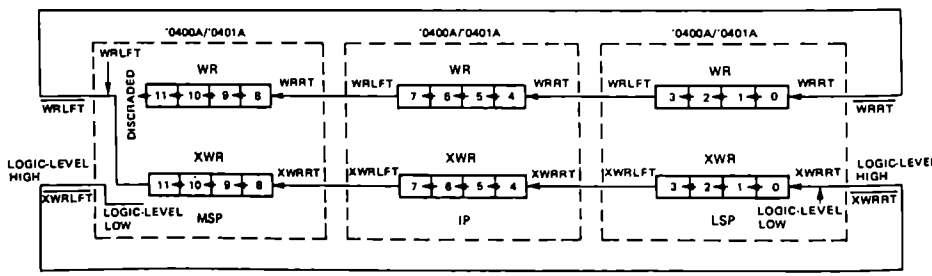


NOTE: WRRT, WRLFT, XWRRT, XWRLFT ARE HIGH-ACTIVE INTRA-PACKAGE AND LOW-ACTIVE (INVERSE POLARITY) INTER-PACKAGE.

FIGURE 14 – RIGHT SHIFT LOGICAL – DOUBLE PRECISION (RSL – DP)

4.2.2 (WR Plus ALUCIN, XWR) LSL → WR,XWR

The WR,XWR double-precision logical left-shift operation, shown in Figure 15, displaces the entire contents of the double length register, formed by the WR in conjunction with the XWR, one bit position to the left. In an expanded wordlength system, the XWR's displaced MSB of the MSP exits the MSP via the bidirectional shift accommodation $\overline{\text{WRLFT}}$ and enters WR's LSB of the LSP via the bidirectional shift accommodation $\overline{\text{WRRT}}$. A logic-level low is automatically left-shifted into the XWR's LSB of the LSP. This logic-level low, sourced by the MSP, exits the MSP via the bidirectional shift accommodation $\overline{\text{XWRLFT}}$ and enters the LSP via the bidirectional shift accommodation $\overline{\text{XWRRT}}$. During each WR,XWR LSL operation, the WR's displaced MSB is discarded.



NOTE: WRRT, WRLFT, XWRRT, XWRLFT ARE HIGH-ACTIVE INTRA-PACKAGE AND LOW-ACTIVE (INVERSE POLARITY) INTER-PACKAGE.

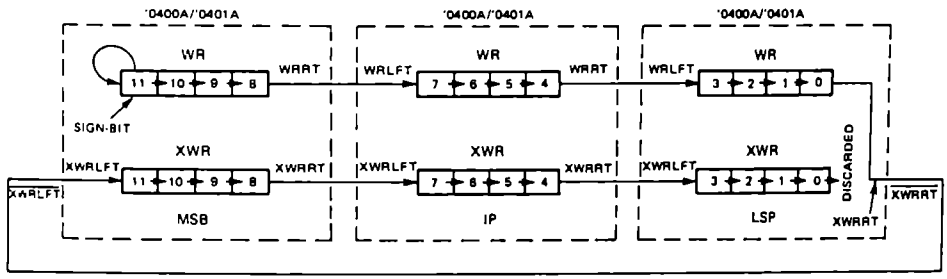
FIGURE 15 – LEFT SHIFT LOGICAL – DOUBLE PRECISION (LSL – DP)

4.2.3 (WR Plus ALUCIN, XWR) RSA → WR,XWR

The WR,XWR double-precision arithmetic right-shift operations, shown in Figures 16 and 17, displace the entire contents of the double-length register, formed by the WR in conjunction with the XWR, one bit position to the right. In an expanded wordlength system, the WR's displaced LSB of the LSP exits the LSP via the bidirectional shift accommodation $\overline{\text{XWRRT}}$ and enters either the XWR's MSB or MSB-minus-1 of the MSP (see 4.2.3.1 and 4.2.3.2). The polarity of the MSP's relative position control input POS0 selects between single-signed and double-signed double-precision arithmetic right-shift operations.

4.2.3.1 Single-Signed Double-Precision RSA (MSP POS0=H)

For the single-signed WR,XWR double-precision right-shift operation, shown in Figure 16, the WR's MSB of the MSP only is designated as a sign-bit. As the entire contents of the WR,XWR is displaced one bit position to the right, the sign-bit does *not* change. Rather, the sign-bit is duplicated to the right. The WR's displaced LSB of the LSP exits the LSP via the bidirectional shift accommodation $\overline{\text{XWRRT}}$ and enters the XWR's MSB of the MSP via the bidirectional shift accommodation $\overline{\text{XWRLFT}}$. The XWR's displaced LSB of the LSP is discarded.

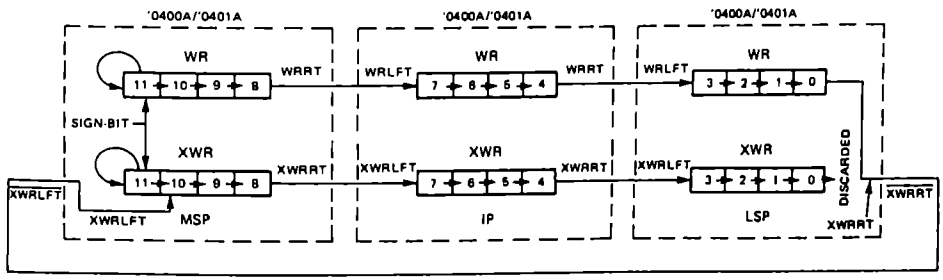


NOTE: WRRT, WRLFT, XWRRT, XWRLFT ARE HIGH-ACTIVE INTRA-PACKAGE AND LOW-ACTIVE (INVERSE POLARITY) INTER-PACKAGE.

FIGURE 16 – RIGHT SHIFT ARITHMETIC – SINGLE SIGN/DOUBLE PRECISION (RSA – SS/DP)

4.2.3.2 Double-Signed Double-Precision RSA (MSP POS0=L)

For the double-signed WR,XWR double-precision right-shift operation, shown in Figure 17, both the WR's and XWR's MSB of the MSP are designated as a sign-bit. As the entire contents of the WR,XWR is displaced one bit position to the right, the sign-bits do not change. Rather, the WR's sign-bit is duplicated to the right while the XWR's sign-bit is held stationary. The WR's displaced LSB of the LSP exits the LSP via the bidirectional shift accommodation $\overline{\text{XWRRT}}$ and enters the XWR's MSB-minus-1 of the MSP via the bidirectional shift accommodation $\overline{\text{XWRLFT}}$. The XWR's displaced LSB of the LSP is discarded.



NOTE: WRRT, WRLFT, XWRRT, XWRLFT ARE HIGH-ACTIVE INTRA-PACKAGE AND LOW-ACTIVE (INVERSE POLARITY) INTER-PACKAGE.

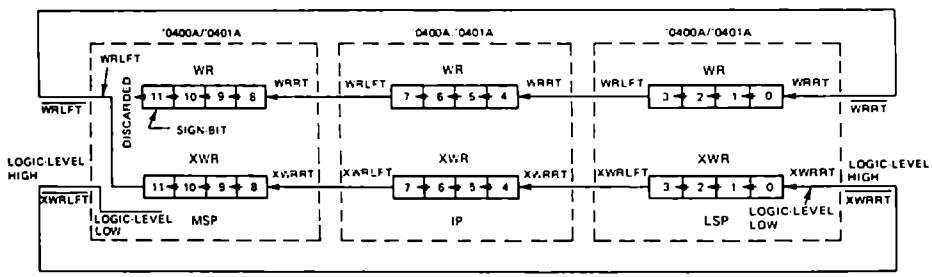
FIGURE 17 – RIGHT SHIFT ARITHMETIC – DOUBLE SIGN/DOUBLE PRECISION (RSA – DS/DP)

4.2.4 (WR Plus ALUCIN, XWR) LSA → WR,XWR

The WR,XWR double-precision arithmetic left-shift operations, shown in Figures 18 and 19, displace the entire contents of the double-length register, formed by the WR in conjunction with the XWR, one bit position to the left. In an expanded wordlength system, either the XWR's displaced MSB or MSB-minus-1 of the MSP exits the MSP via the bidirectional shift accommodation $\overline{\text{WRLFT}}$ and enters the WR's LSB of the LSP via the bidirectional shift accommodation $\overline{\text{WRRT}}$. The polarity of the MSP's relative position control input POS0 selects between single-signed and double-signed double-precision arithmetic left-shift operations.

4.2.4.1 Single-Signed Double-Precision LSA (MSP POS0=H)

The single-signed WR,XWR double-precision arithmetic left-shift operation, shown in Figure 18, is functionally identical to the WR,XWR double-precision logical left-shift operation. The WR's MSB of the MSP, although designated as a sign-bit, is discarded as the entire contents of the double-length WR,XWR register is displaced one bit position to the left. As each WR,XWR LSA operation is performed, the BMSB output (WR sign bit) may be compared to the MSB of the MSP's DOP (data displacing into WR sign bit) to detect an impending change in WR sign bit polarity.

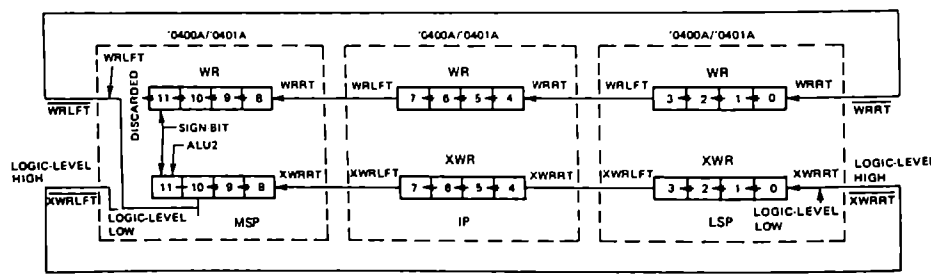


NOTE: WRRT, WRLFT, XWRRT, XWRLFT ARE HIGH-ACTIVE INTRA-PACKAGE AND LOW-ACTIVE (INVERSE POLARITY) INTER-PACKAGE.

FIGURE 18 – LEFT SHIFT ARITHMETIC – SINGLE SIGN/DOUBLE PRECISION (LSA – SS/DP)

4.2.4.2 Double-Signed Double-Precision LSA (MSP POS0=L)

The double-signed WR,XWR double-precision arithmetic left-shift operation shown in Figure 19 is, with one exception, functionally identical to the WR,XWR double-precision left-shift operation. The exception is, the XWR's sign-bit is automatically forced to the polarity of the MSP's ALU2 output. As each double-signed double-precision LSA operation is performed, the WR's sign-bit is discarded. Consequently the BMSB output (WR sign bit) may be compared to the MSB of the MSP's DOP (ALU2 data displacing into WR sign bit) to detect an impending change in WR sign bit polarity.

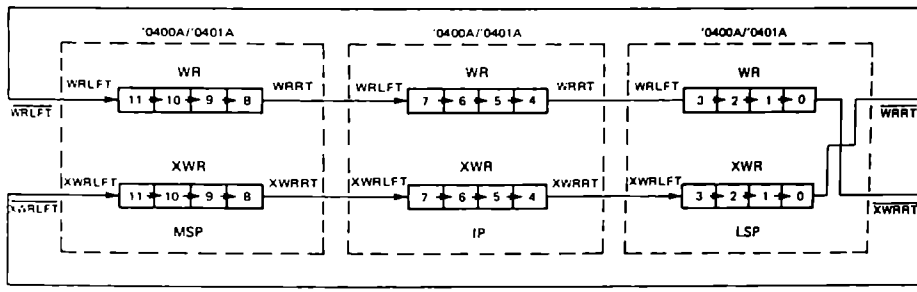


NOTE: WRRT, WRLFT, XWRRT, XWRLFT ARE HIGH-ACTIVE INTRA-PACKAGE AND LOW-ACTIVE (INVERSE POLARITY) INTER-PACKAGE.

FIGURE 19 – LEFT SHIFT ARITHMETIC – DOUBLE SIGN/DOUBLE PRECISION (LSA – DS/DP)

4.2.5 (WR Plus ALUCIN, XWR) RCIR → WR,XWR

The WR,XWR double-precision right-circulate operation, shown in Figure 20, displaces the entire contents of the double-length register, formed by the WR in conjunction with the XWR, one bit position to the right. In an expanded wordlength system, the WR's displaced LSB of the LSP exits the LSP via the bidirectional shift accommodation $\overline{\text{XWRRT}}$ and enters the XWR's MSB of the MSP via the bidirectional shift accommodation $\overline{\text{XWRLFT}}$. The XWR's LSB of the LSP exits the LSP via the bidirectional shift accommodation $\overline{\text{WRRT}}$ and enters the WR's MSB of the MSP via the bidirectional shift accommodation $\overline{\text{WRLFT}}$.

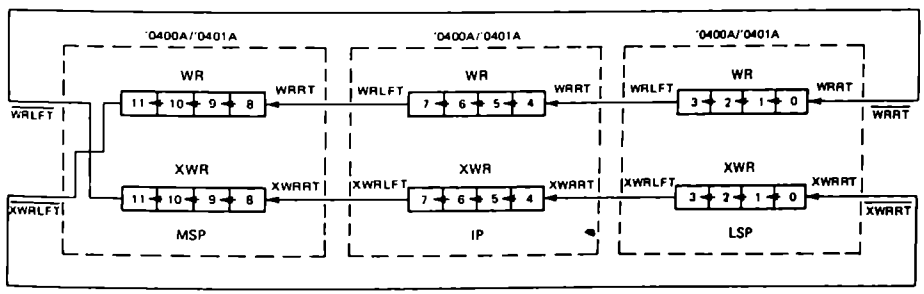


NOTE: WRRT, WRLFT, XWRRT, XWRLFT ARE HIGH-ACTIVE INTRA-PACKAGE AND LOW-ACTIVE (INVERSE POLARITY) INTER-PACKAGE.

FIGURE 20 – RIGHT CIRCULATE – DOUBLE PRECISION (RCIR – DP)

4.2.6 (WR Plus ALUCIN, XWR) LCIR → WR,XWR

The WR,XWR double-precision left-circulate operation, shown in Figure 21, displaces the entire contents of the double-length register, formed by the WR in conjunction with the XWR, one bit position to the left. In an expanded wordlength system, the WR's displaced MSB of the MSP exits the MSP via the bidirectional shift accommodation $\overline{\text{XWRLFT}}$ and enters the XWR's LSB of the LSP via the bidirectional shift accommodation $\overline{\text{XWRRT}}$. The XWR's MSB of the MSP exits the MSP via the bidirectional shift accommodation $\overline{\text{WRLFT}}$ and enters the WR's LSB of the LSP via the bidirectional shift accommodation $\overline{\text{WRRT}}$.



NOTE: WRRT, WRLFT, XWRRT, XWRLFT ARE HIGH-ACTIVE INTRA-PACKAGE AND LOW-ACTIVE (INVERSE POLARITY) INTER-PACKAGE.

FIGURE 21 – LEFT CIRCULATE – DOUBLE PRECISION (LCIR – DP)

4.3 COMPOUND-FUNCTION WR,XWR DOUBLE-PRECISION SHIFTS/CIRCULATES

Compound-function WR,XWR double-precision shift/circulate operations extend the processing power of the basic double-precision RSA and LCIR operations to boost systems-level efficiency in the assembly of iterative macro-instructions such as multiply and non-restoring divide. These compound-function shift/circulate operations, directed by the resident operation with expanded wordlength "end" conditions handled by the relative position controls, may best be represented by the generalized symbol:

(WR plus/minus A plus ALUCIN, XWR) RSA/LCIR → WR,XWR
where A is either the DIP or RF

Within a single microcycle, each of eight possible compound-function WR,XWR double-precision shift/circulate operations is capable of 1) asynchronously summing/subtracting either the RF or DIP with/from the WR, then 2) asynchronously adding the result to the ALUCIN input, then 3) asynchronously double-precision shifting/circulating (RSA/LCIR) the result with the WR and XWR considered as one double-length register, and finally 4) synchronously storing the shifted/circulated result into the double-length register formed by the WR in conjunction with the XWR. The eight compound-function WR,XWR double-precision shift/circulate possibilities, with data flow paths for expanded wordlengths, are listed in Table 19.

TABLE 19
COMPOUND-FUNCTION WR, XWR
DOUBLE-PRECISION SHIFTS/CIRCULATES

SHIFT/CIRCULATE OPERATION	SHIFT/CIRCULATE FUNCTION	EXPANDED WORDLENGTH DATA FLOW PATHS	OP-FORM (See 5.3)	OP-FIELD OP3 - OP0	D-FIELD D1 - D0	S-FIELD S2 → S0
(WR minus DIP minus 1 plus ALUCIN, XWR) LCIR → WR, XWR	LEFT-CIRCULATE (LCIR)	Figure 21	IVa	HLLL	HH	LHL
(WR minus RF(n) minus 1 plus ALUCIN, XWR) LCIR → WR, XWR	LEFT-CIRCULATE (LCIR)	Figure 21	IVc	HLLL	HL	LLL → HHH
(WR plus DIP plus ALUCIN, XWR) LCIR → WR, XWR	LEFT-CIRCULATE (LCIR)	Figure 21	IVb	HLLH	HH	LHL
(WR plus RF(n) plus ALUCIN, XWR) LCIR → WR, XWR	LEFT-CIRCULATE (LCIR)	Figure 21	IVd	HLLH	HL	LLL → HHH
(WR minus DIP minus 1 plus ALUCIN, XWR) RSA → WR, XWR	RIGHT-SHIFT-ARITHMETIC (RSA)	Figure 16	IVf	LLHL	HH	LHL
(WR minus RF(n) minus 1 plus ALUCIN, XWR) RSA → WR, XWR	RIGHT-SHIFT-ARITHMETIC (RSA)	Figure 16	IVh	LLHL	HL	LLL → HHH
(WR plus DIP plus ALUCIN, XWR) RSA → WR, XWR	RIGHT-SHIFT-ARITHMETIC (RSA)	Figure 16	IVg	HLHH	HH	LHL
(WR plus RF(n) plus ALUCIN, XWR) RSA → WR, XWR	RIGHT-SHIFT-ARITHMETIC (RSA)	Figure 16	IVi	HLHH	HL	LLL → HHH

5. OPERATION SET (MICROINSTRUCTION SET)

The SBP0400A and SBP0401A are supplied with an identical set of 459 non-redundant standard factory-defined operations (microinstructions). The only difference between the SBP0400A and the SBP0401A is the presence and absence of the operation register (OR):

a. The SBP0400A contains a 20-bit operation register. After the 9-bit operation code is applied (and setup), the positive-going clock transition causes the resident operation to be stored in the OR. See Figure 5 and microinstruction overlap, paragraph 5.1.

b. The SBP0401A, without the OR, derives its resident operation from a steady-state 9-bit code applied at the operation select inputs. See Figure 5.

5.1 SBP0400A MICROINSTRUCTION OVERLAP

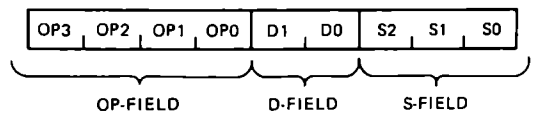
Within a single microcycle (1 clock period), any one of the '0400A's 459 unique operations may be both selected and executed. While the "present" microinstruction is directing the '0400A's functional blocks and data paths from the OR, the "next" microinstruction may be setup for entry into the OR. As the results of the "present" microinstruction are synchronously stored at their appointed destination, the "next" microinstruction simultaneously enters the OR where it becomes the "present" microinstruction. This technique of overlapping microinstruction setup with microinstruction execution (Figure 5) allows a string of successive microinstructions to be executed, one each, during successive microcycles.

5.2 OPERATION-SELECT WORD

Each of the 459 operations is selected by presenting 9-bits of encoded microinstruction data to the operation-select input lines which is then asynchronously decoded/translated by the PLA. In the SBP0400A this decoded/translated microinstruction enters the OR synchronous with the completion of the previous microinstruction (positive transition of the clock) to become the resident operation. In the SBP0401A this decoded/translated microinstruction is distributed directly from the 20 outputs of the PLA as the resident operation.

The 9-bit operation-select word is partitioned, as shown below, into three interacting fields: 1) the 2-bit D-field, 2) the 4-bit OP-field, and 3) the 3-bit S-field.

OPERATION-SELECT WORD

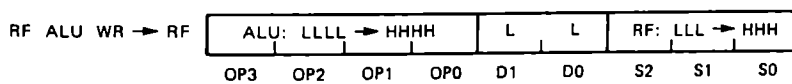


5.2.1 D-Field, Operation-Select Word

This 2-bit D-field (D1 → D0) of the operation-select word governs the manner in which the OP-field and S-field are interpreted to specify the operations. Four D-field possibilities exist. They are: LL, LH, HL, and HH.

5.2.1.1 D-Field = LL

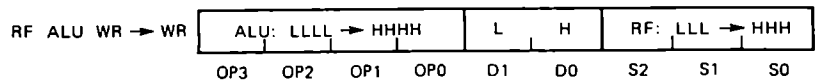
When the D-field is "LL", the RF and WR, as shown below, are designated as operand sources with the RF also designated as the operation-result destination.



The 3-bit S-field is interpreted to select 1 of 8 RF locations both as an operand source and an operation-result destination; the 4-bit OP-field is interpreted to select one of 16 ALU functions (micro-operations) as the operand combination/modification mechanism.

5.2.1.2 D-Field = LH

When the D-field is "LH", the RF and WR, as shown below, are designated as operand sources with the WR also designated as the operation-result destination.



The 3-bit S-field is interpreted to select 1 of 8 RF locations as an operand source, the 4-bit OP-field is interpreted to select one of 16 ALU functions (micro-operations) as the operand combination/modification mechanism.

5.2.1.3 D-Field = HL

When the D-field is "HL", the ALU functions (micro-operations) available for the combination/modification of operands are limited to 1) plus, 2) minus, or 3) unconditional ALU-bypass (no ALU function)

As shown in Table 20, the 3-bit S-field is primarily interpreted to select one of eight RF locations as an operand source and/or operation-result destination; the 4-bit OP-field is interpreted to select a limited ALU function in conjunction with an operand source and/or operand-result destination.

TABLE 20
D-FIELD = HL

	OP3	OP2	OP1	OP0	D1	D0	S2 S1 S0
RF → DOP	L	L	L	L	H	L	RF: LLL → HHH
RF + XWR	L	L	L	H	H	L	RF: LLL + HHH
(WR minus RF minus 1 plus ALUCIN, XWR) RSA → WR, XWR	L	L	H	L	H	L	RF: LLL → HHH
RF plus WR plus ALUCIN + XWR	L	L	H	H	H	L	RF: LLL + HHH
RF plus DIP plus ALUCIN → WR	L	H	L	L	H	L	RF: LLL → HHH
RF plus DIP plus ALUCIN → XWR	L	H	L	H	H	L	RF: LLL → HHH
DIP → WR	L	H	H	L	H	L	Don't Care X X X
RF plus DIP plus ALUCIN → RF	L	H	H	H	H	L	RF: LLL → HHH
(WR minus RF minus 1 plus ALUCIN, XWR) LCIR → WR, XWR	H	L	L	L	H	L	RF: LLL → HHH
(WR plus RF plus ALUCIN, XWR) LCIR → WR, XWR	H	L	L	H	H	L	RF: LLL → HHH
(WR plus ALUCIN, XWR) RSA → WR, XWR	H	L	H	L	H	L	Don't Care X X X
(WR plus RF plus ALUCIN) RSA → WR, XWR	H	L	H	H	H	L	RF: LLL → HHH
RF plus XWR plus ALUCIN → WR	H	H	L	L	H	L	RF: LLL → HHH
RF plus XWR plus ALUCIN → XWR	H	H	L	H	H	L	RF: LLL → HHH
XWR plus ALUCIN → RF	H	H	H	L	H	L	RF: LLL → HHH
DIP → RF	H	H	H	H	H	L	RF: LLL → HHH
	OP3	OP2	OP1	OP0	D1	D0	S2 S1 S0

5.2.1.4 D-Field = HH

When the D-field is "HH", the RF is neither used as an operand source nor an operation-result destination. Rather, two S-field possibilities (LHL, HLH) are, as shown in Table 21, interpreted to extend the 4-bit OP-field to select one of 32 non-RF operations. The extended OP-field is interpreted to select a limited ALU function in conjunction with an operand source(s) and an operation-result destination.

TABLE 21
D-FIELD = HH

	OP3	OP2	OP1	OP0	D1	D0	S2	S1	S0
DIP → DOP	L	L	L	L	H	H	L	H	L
DIP → XWR	L	L	L	H	H	H	L	H	L
(WR minus DIP minus 1 plus ALUCIN, XWR) RSA → WR, XWR	L	L	H	L	H	H	L	H	L
DIP plus WR plus ALUCIN → XWR	L	L	H	H	H	H	L	H	L
$F_{1,}$ plus ALUCIN → DOP	L	H	L	L	H	H	L	H	L
DIP plus WR plus ALUCIN → DOP	L	H	L	H	H	H	L	H	L
DIP → WR	L	H	H	L	H	H	L	H	L
DIP plus WR plus ALUCIN → DOP	L	H	H	H	H	H	L	H	L
(WR minus DIP minus 1 plus ALUCIN, XWR) LCIR → WR, XWR	H	L	L	L	H	H	L	H	L
(WR plus DIP plus ALUCIN, XWR) LCIR → WR, XWR	H	L	L	H	H	H	L	H	L
(WR plus ALUCIN, XWR) RSA → WR, XWR	H	L	H	L	H	H	L	H	L
(WR plus DIP plus ALUCIN, XWR) RSA → WR, XWR	H	L	H	H	H	H	L	H	L
DIP plus XWR plus ALUCIN → WR	H	H	L	L	H	H	L	H	L
DIP plus XWR plus ALUCIN → XWR	H	H	L	H	H	H	L	H	L
XWR plus ALUCIN → DOP	H	H	H	L	H	H	L	H	L
DIP → DOP	H	H	H	H	H	H	L	H	L

	OP3	OP2	OP1	OP0	D1	D0	S2	S1	S0
(WR plus ALUCIN) RSA → WR	L	L	L	L	H	H	H	L	H
(WR plus ALUCIN) RCIR → WR	L	L	L	H	H	H	H	L	H
(WR plus ALUCIN) LSA → WR	L	L	H	L	H	H	H	L	H
(WR plus ALUCIN) LCIR → WR	L	L	H	H	H	H	H	L	H
(WR plus ALUCIN, XWR) RSA → WR, XWR	L	H	L	L	H	H	H	L	H
(WR plus ALUCIN, XWR) RCIR → WR, XWR	L	H	L	H	H	H	H	L	H
(WR plus ALUCIN, XWR) LSA → WR, XWR	L	H	H	L	H	H	H	L	H
(WR plus ALUCIN, XWR) LCIR → WR, XWR	L	H	H	H	H	H	H	L	H
(WR plus ALUCIN)RSL → WR	H	L	L	L	H	H	H	L	H
(WR plus ALUCIN) RCIR → WR	H	L	L	H	H	H	H	L	H
(WR plus ALUCIN) LSL → WR	H	L	H	L	H	H	H	L	H
(WR plus ALUCIN) LCIR → WR	H	L	H	H	H	H	H	L	H
(WR plus ALUCIN, XWR) RSL → WR, XWR	H	H	L	L	H	H	H	L	H
(WR plus ALUCIN, XWR) RCIR → WR, XWR	H	H	L	H	H	H	H	L	H
(WR plus ALUCIN, XWR) LSL → WR, XWR	H	H	H	L	H	H	H	L	H
(WR plus ALUCIN, XWR) LCIR → WR, XWR	H	H	H	H	H	H	H	L	H

OP3	OP2	OP1	OP0	D1	D0	S2	S1	S0

5.2.2 OP-Field, Operation-Select Word

The 4-bit OP-field (OP3 → OP0) of the operation-select word interacts with the D-field and S-field to specify an ALU function as the operand combination/modification mechanism for operations (microinstructions).

5.2.2.1 OP-Field ALU Function (Micro-Operation) Selection

The most consistent utilization of the OP-field is realized when specifying one of 16 ALU functions, listed in Table 22, as the operand combination/modification mechanism for those particular operations listed in Table 23. For those

TABLE 22
ALU FUNCTION (MICRO-OPERATION SELECT)

ALU OP-FIELD				ACTIVE-HIGH DATA	
				ALUCIN = H	ALUCIN = L
OP3	OP2	OP1	OP0	(WITH CARRY)	(NO CARRY)
L	L	L	L	Fn = L	Fn = H
L	L	L	H	Fn = B minus A	Fn = B minus A minus 1
L	L	H	L	Fn = A minus B	Fn = A minus B minus 1
L	L	H	H	Fn = A plus B plus 1	Fn = A plus B
L	H	L	L	Fn = B plus 1	Fn = B
L	H	L	H	Fn = $\overline{B}$ plus 1	Fn = $\overline{B}$
L	H	H	L	Fn = A plus 1	Fn = A
L	H	H	H	Fn = $\overline{A}$ plus 1	Fn = $\overline{A}$
H	L	L	L	Fn = AnBn	
H	L	L	H	Fn = An ⊙ Bn	
H	L	H	L	Fn = $\overline{An \odot Bn}$	
H	L	H	H	Fn = $\overline{A}$nBn	
H	H	L	L	Fn = An$\overline{B}$n	
H	H	L	H	Fn = An + $\overline{B}$n	
H	H	H	L	Fn = $\overline{A}$n + Bn	
H	H	H	H	Fn = An + Bn	

TABLE 23
16 FUNCTION ALU OPERATIONS

	OP3 → OP0	D1	D0	S2	S1	S0
RF ALU WR → RF	ALU: LLLL → HHHH	L	L	RF: LLL → HHH		
RF ALU WR → WR	ALU: LLLL → HHHH	L	H	RF: LLL → HHH		
*DIP ALU WR → DOP	ALU: LLLL → HHHH	H	H	L	L	L
*DIP ALU WR → WR	ALU: LLLL → HHHH	H	H	L	L	H
DIP ALU XWR → WR	ALU: LLLL → HHHH	H	H	L	H	H
DIP ALU WR → XWR	ALU: LLLL → HHHH	H	H	H	L	L
DIP ALU XWR → XWR	ALU: LLLL → HHHH	H	H	H	H	L
DIP ALU XWR → DOP	ALU: LLLL → HHHH	H	H	H	H	H

NOTE: When PC PRIORITY is low WR → AOP
*XWR → AOP

operations, the D-field interacts with the S-field to specify two operand sources in combination with an operation-result destination. Either the DIP or RF is available as an operand source to the "A" input port of the ALU; either the DIP, WR or XWR is available as an operand source to the "B" input port of the ALU. Ultimate destinations for ALU output results include either the DOP, RF, WR or XWR.

An ALU function from Table 22 may be selected as the operand combination/modification mechanism for each operation in Table 23 by simply choosing the appropriate OP-field code. For example, a D-field code of "HH" interacts with an S-field code of "LLH" to specify the operation DIP ALU WR → WR. If the WR is to be subtracted from the DIP, an OP-field code of "LLHL" (F_n = A minus B, ALUCIN = H) must be selected from Table 22 along with an ALUCIN = H forced into the LSP. The resulting operation-select word will then specify the operation DIP minus WR → DOP.

OP	D	S
LLHL	HH	LLL

An OP-field choice of "LLLH" would automatically interchange the operands and specify the operation WR minus DIP → DOP. In fact, any of eight arithmetic or eight Boolean ALU functions may be selected from Table 22 and impressed upon any operation in Table 23.

Although the ALU generally accepts two operand sources simultaneously as inputs, certain ALU functions may be selected from Table 22 which only consider one operand source. These ALU functions, when impressed upon the operations of Table 23, specify the register transfer operations of Table 24. These register transfer operations allow: 1) unconditioned transfers, X → Y with the LSP's ALUCIN = L, 2) incrementing transfers, X plus 1 → Y with the LSP's ALUCIN = H, 3) one's-complement transfers, $\overline{X}$ → Y with the LSP's ALUCIN = L, and 4) two's-complement transfers, $\overline{X}$ plus 1 → Y with the LSP's ALUCIN = H.

TABLE 24
REGISTER TRANSFER OPERATIONS

	OP3	OP2	OP1	OP0	D1	D0	S2 S1 S0
WR plus ALUCIN → RF	L	H	L	L	L	L	RF: LLL → HHH
RF plus ALUCIN → WR	L	H	H	L	L	H	RF: LLL → HHH
WR plus ALUCIN → XWR	L	H	L	L	H	H	H L L
XWR plus ALUCIN → WR	L	H	L	L	H	H	L H H
DIP plus ALUCIN → WR	L	H	H	L	H	H	L H H
DIP plus ALUCIN → XWR	L	H	H	L	H	H	H L L
DIP plus ALUCIN → DOP	L	H	H	L	H	H	H H H
XWR plus ALUCIN → DOP	L	H	L	L	H	H	H H H
*DIP plus ALUCIN → DOP	L	H	H	L	H	H	L L L
*WR plus ALUCIN → DOP	L	H	L	L	H	H	L L L
DIP plus ALUCIN → WR	L	H	H	L	H	H	L L H
	OP3	**OP2**	**OP1**	**OP0**	**D1**	**D0**	**S2 S1 S0**
$\overline{WR}$ plus ALUCIN → RF	L	H	L	H	L	L	RF: LLL → HHH
$\overline{RF}$ plus ALUCIN → WR	L	H	H	H	L	H	RF: LLL → HHH
$\overline{WR}$ plus ALUCIN → XWR	L	H	L	H	H	H	H L L
$\overline{XWR}$ plus ALUCIN → WR	L	H	L	H	H	H	L H H
$\overline{DIP}$ plus ALUCIN → WR	L	H	H	H	H	H	L H H
$\overline{DIP}$ plus ALUCIN → XWR	L	H	H	H	H	H	H L L
$\overline{DIP}$ plus ALUCIN → DOP	L	H	H	H	H	H	H H H
$\overline{XWR}$ plus ALUCIN → DOP	L	H	L	H	H	H	H H H
*$\overline{DIP}$ plus ALUCIN → DOP	L	H	H	H	H	H	L L L
*$\overline{WR}$ plus ALUCIN → DOP	L	H	L	H	H	H	L L L
*$\overline{DIP}$ plus ALUCIN → WR	L	H	H	H	H	H	L L H
	OP3	**OP2**	**OP1**	**OP0**	**D1**	**D0**	**S2 S1 S0**

* XWR → AOP, otherwise WR → AOP. PC PRIORITY overrides.

Certain ALU functions may be selected from Table 22 to facilitate register "clear" (all logic-level LOWs) and register "preset" (all logic-level HIGHs) operations. These ALU functions, when impressed upon the operations of Table 23, specify the register "clear" and "preset" operations of Table 25.

TABLE 25
REGISTER CLEAR AND PRESET OPERATIONS

	OP3	OP2	OP1	OP0	D1	D0	S2 S1 S0
LOW → RF, ALUCIN = HIGH	L	L	L	L	L	L	RF: LLL → HHH
LOW → WR, ALUCIN = HIGH	L	L	L	L	H	H	L H H
*LOW → WR, ALUCIN = HIGH	L	L	L	L	H	H	L L H
LOW → XWR, ALUCIN = HIGH	L	L	L	L	H	H	H H L
LOW → DOP, ALUCIN = HIGH	L	L	L	L	H	H	H H H
*LOW → DOP, ALUCIN = HIGH	L	L	L	L	H	H	L L L
	OP3	OP2	OP1	OP0	D1	D0	S2 S1 S0
HIGH → RF, ALUCIN = LOW	L	L	L	L	L	L	RF: LLL → HHH
HIGH → WR, ALUCIN = LOW	L	L	L	L	H	H	L H H
*HIGH → WR, ALUCIN = LOW	L	L	L	L	H	H	L L H
HIGH → XWR, ALUCIN = LOW	L	L	L	L	H	H	H H L
HIGH → DOP, ALUCIN = LOW	L	L	L	L	H	H	H H H
*HIGH → DOP, ALUCIN = LOW	L	L	L	L	H	H	L L L
	OP3	OP2	OP1	OP0	D1	D0	S2 S1 S0

* XWR → AOP, otherwise WR → AOP. PC PRIORITY = HIGH overrides

5.2.2.2 OP-Field Operand-Source/ALU Function/Operation-Result-Destination Selection

The 4-bit OP-field also interacts with the D-field and S-field to specify the operations of Tables 22 and 23. For these operations, the ALU functions available for operand combination/modification are limited to: 1) plus, 2) minus, and 3) unconditioned ALU-bypass (no ALU functions).

5.2.3 S-Field, Operation-Select Word

The 3-bit S-field (S2 → S0) of the operation-select word either: 1) specifies one of eight RF locations, shown in Table 26, as an operand source and/or operation-result destination, or 2) extends the 4-bit OP-field to select one of 32 non-RF operations as listed in Table 23.

TABLE 26
RF SELECTION

RF LOCATION	S2	S1	S0
RF0	L	L	L
RF1	L	L	H
RF2	L	H	L
RF3	L	H	H
RF4	H	L	L
RF5	H	L	H
RF6	H	H	L
RF7 (PC)	H	H	H

NOTE: D-FIELD is LL, LH, or HL

5.3 INDEX TO MICROINSTRUCTIONS BY OPERATION FORM

The operation (microinstruction) set may be sectioned into six operation-forms as described in Tables 27 through 32. Each operation-form may, in turn, be subsequently sectioned into a group of operation-types. In general, for each operation type, the WR is automatically selected by the OR to source the AOP via the ADR MUX. The exception to this statement is realized in operation-form I, operation-types a and b where the XWR is automatically selected by the OR to source the AOP via the ADR MUX. Of course, when the PC PRIORITY input is taken to a logic-level high, OR selection of the ADR MUX is overridden. In this situation, the PC is prioritized to source the AOP via the ADR MUX.

In general, the execution results of most operations may be monitored at the DOP whether the result destination is the RF, WR, XWR or DOP itself. The only exceptions are realized when the DOB is not involved in operation execution. These exceptions include the DIP → WR transfer of operation-form III operation-type d, and the XWR portion of the double-precision shift/circulates involved throughout operation-forms IV and VI.

5.3.1 Operation – Form I

Operation form I may be utilized to perform one of 16 ALU functions, selected by the Operation-Select Word OP-field, on two of four operand sources, (RF, WR, XWR, DIP). The result is transferred to one of four operation-result destinations (RF, WR, XWR, DOP).

TABLE 27
OPERATION FORM I

I	OPERATION TYPE	OP3 -- OP0	D1	D0	S2	S1	S0
a.	RF ALU WR - RF	ALU: LLLL → HHHH	L	L	RF: LLL → HHH		
b.	RF ALU WR - WR	ALU: LLLL → HHHH	L	H	RF: LLL → HHH		
c.	*DIP ALU WR → DOP	ALU: LLLL → HHHH	H	H	L	L	L
d.	*DIP ALU WR → WR	ALU: LLLL → HHHH	H	H	L	L	H
e.	DIP ALU XWR - WR	ALU: LLLL → HHHH	H	H	L	H	H
f.	DIP ALU WR → XWR	ALU: LLLL → HHHH	H	H	H	L	L
g.	DIP ALU XWR → XWR	ALU: LLLL → HHHH	H	H	H	H	L
h.	DIP ALU XWR → DOP	ALU: LLLL → HHHH	H	H	H	H	H

*XWR → AOP, otherwise WR → AOP. PC PRIORITY - HIGH overrides

5.3.2 Operation – Form II

Operation form II may be utilized to arithmetically sum one or two operand sources (RF, WR, XWR, DIP) and a ripple-carry-in (ALUCIN). The operation-result is transferred to one of four destinations (RF, WR, XWR, DOP).

TABLE 28
OPERATION FORM II

II	OPERATION TYPE	OP3 → OP0	D1	D0	S2	S1	S0
a.	RF plus WR plus ALUCIN → XWR	L L H H	H	L	RF: LLL → HHH		
b.	RF plus DIP plus ALUCIN - WR	L H L L	H	L	RF: LLL → HHH		
c.	RF plus DIP plus ALUCIN → XWR	L H L H	H	L	RF: LLL → HHH		
d.	RF plus DIP plus ALUCIN → RF	L H H H	H	L	RF: LLL → HHH		
e.	RF plus XWR plus ALUCIN → WR	H H L L	H	L	RF: LLL → HHH		
f.	RF plus XWR plus ALUCIN → XWR	H H L H	H	L	RF: LLL → HHH		
g.	XWR plus ALUCIN → RF	H H H L	H	L	RF: LLL → HHH		
h.	DIP plus WR plus ALUCIN → XWR	L L H H	H	H	L	H	L
i.	DIP plus WR plus ALUCIN → DOP	L H H H	H	H	L	H	L
j.	DIP plus XWR plus ALUCIN → WR	H H L L	H	H	L	H	L
k.	DIP plus XWR plus ALUCIN → XWR	H H L H	H	H	L	H	L
l.	XWR plus ALUCIN → DOP	H H H L	H	H	L	H	L

NOTE: When PC PRIORITY is LOW, WR → AOP

5.3.3 Operation – Form III

Operation form III may be utilized to transfer one or two operand sources (RF, DIP) to one of four destinations (RF, WR, XWR, DOP).

TABLE 29
OPERATION FORM III

III	OPERATION TYPE	OP3 → OP0	D1	D0	S2	S1	S0
a.	DIP → RF	H H H H	H	L	RF: LLL → HHH		
b.	RF → DOP	L L L L	H	L	RF: LLL → HHH		
c.	RF → XWR	L L L H	H	L	RF: LLL → HHH		
d.	DIP → WR	L H H L	H	L	X	X	X
		L H H L	H	H	L	H	L
e.	DIP → XWR	L L L H	H	H	L	H	L
f.	DIP → DOP	H H H H	H	H	L	H	L
		L L L L	H	H	L	H	L

NOTE: When PC PRIORITY is LOW, WR → AOP

5.3.4 Operation – Form IV

Operation form IV may be utilized to either:

- arithmetically sum the WR and the ripple carry-in (ALUCIN) with one of two operand sources (RF, DIP), arithmetically double-precision shift the result to the right, and transfer the shifted result to the WR and XWR;
- arithmetically sum the WR and the ripple carry-in (ALUCIN) with one of two operand sources (RF, DIP), double-precision circulate the result to the left, and transfer the circulated result to the WR and XWR;
- arithmetically subtract one of two operand sources (RF, DIP) and −1 from the WR, arithmetically add the ripple carry-in (ALUCIN), double-precision circulate the result to the left, and transfer the circulated result to the WR and XWR;
- arithmetically subtract one of two operand sources (RF, DIP) and −1 from the WR, arithmetically add the ripple carry-in (ALUCIN), arithmetically double-precision shift the result to the right and transfer the shifted result to the WR and XWR.

TABLE 30
OPERATION FORM IV

IV	OPERATION TYPE	OP3	·		OP0	D1	D0	S2	S1	S0
a.	(WR minus DIP minus 1 plus ALUCIN, XWR) LCIR → WR, XWR	H	L	L	L	H	H	L	H	L
b.	(WR plus DIP plus ALUCIN, XWR) LCIR → WR, XWR	H	L	L	H	H	H	L	H	L
c.	(WR minus RF minus 1 plus ALUCIN, XWR) LCIR → WR, XWR	H	L	L	L	H	L	RF	LLL → HHH	
d.	(WR plus RF plus ALUCIN, XWR) LCIR → WR, XWR	H	L	L	H	H	L	RF	LLL → HHH	
e.	(WR plus ALALUCIN, XWR) RSA → XWR	H	L	H	L	H	L	X	X	X
		H	L	H	L	H	H	L	H	L
f.	(WR minus DIP minus 1 plus ALUCIN, XWR) RSA → WR, XWR	L	L	H	L	H	H	L	H	L
g.	(WR plus DIP plus ALUCIN, XWR) RSA → WR, XWR	H	L	H	H	H	H	L	H	L
h.	(WR minus RF minus 1 plus ALUCIN, XWR) RSA → WR, XWR	L	L	H	L	H	L	RF	LLL → HHH	
i.	(WR plus RF plus ALUCIN, XWR) RSA → WR, XWR	H	L	H	H	H	L	RF	LLL → HHH	

NOTE When PC PRIORITY is LOW, WR → AOP

5.3.5 Operation – Form V

Operation form V may be utilized to perform single-precision shifts on the contents of the WR, placing the result in the WR. The WR may be logically shifted left or right (LSL, RSL), arithmetically shifted left or right (LSA, RSA), or circulated left or right (LCIR, RCIR).

As the WR is passed through the ALU during form V and VI, the ALUCIN is active and should be held at a low logic level for true shifts.

TABLE 31
OPERATION FORM V

V	OPERATION TYPE	OP3 → OP0	D1	D0	S2	S1	S0
a.	(WR plus ALUCIN) RSA → WR	L L L L	H	H	H	L	H
b.	(WR plus ALUCIN) RCIR → WR	L L L H	H	H	H	L	H
		H L L H	H	H	H	L	H
c.	(WR plus ALUCIN) LSA → WR	L L H L	H	H	H	L	H
d.	(WR plus ALUCIN) LCIR → WR	L L H H	H	H	H	L	H
		H L H H	H	H	H	L	H
e	(WR plus ALUCIN) RSL → WR	H L L L	H	H	H	L	H
f.	(WR plus ALUCIN) LSL → WR	H L H L	H	H	H	L	H

NOTE: When PC PRIORITY is LOW, WR → AOP

5.3.6 Operation – Form VI

Operation form VI may be utilized to perform double-precision shifts on the contents of WR in conjunction with XWR. The WR in conjunction with the XWR may be:

- logically shifted left or right (LSL, RSL);
- arithmetically shifted left or right (LSA, RSA) single- or double-signed;
- circulated left or right (LCIR, RCIR).

TABLE 32
OPERATION FORM VI

VI	OPERATION TYPE	OP3 → OP0	D1	D0	R2	R1	R0
a.	(WR plus ALUCIN, XWR) RSA → (WR, XWR)	L H L L	H	H	H	L	H
b.	(WR plus ALUCIN, XWR) RCIR → (WR, XWR)	L H L H H H L H	H H	H H	H H	L L	H H
c.	(WR plus ALUCIN, XWR) LSA → (WR, XWR)	L H H L	H	H	H	L	H
d.	(WR plus ALUCIN, XWR) LCIR → (WR, XWR)	L H H H H H H H	H H	H H	H H	L L	H H
e.	(WR plus ALUCIN, XWR) RSL → (WR, XWR)	H H L L	H	H	H	L	H
f.	(WR plus ALUCIN, XWR) LSL → (WR, XWR)	H H H L	H	H	H	L	H

NOTE: When PC PRIORITY is LOW, WR = DOP

5.4 INDEX TO MICROINSTRUCTIONS BY SOURCE OPERANDS

When the source operand is known, tables 33 through 36 can be used to obtain the form/type and microcode of the possible operations for that source operand.

TABLE 33
DIP SOURCE OPERANDS

OPERATION	OP FORM/TYPE	OP3 – OP0 OP FIELD	D1 D0 D-FIELD	S2 – S0 S-FIELD
DIP → DOP	IIIf	HHHH	HH	LHL
DIP → DOP	IIIf	LLLL	HH	LHL
DIP → RF	IIIa	HHHH	HL	LLL – HHH
DIP → WR	IIId	LHHL	HL	XXX
DIP → WR	IIId	LHHL	HH	LHL
DIP → XWR	IIIe	LLLH	HH	LHL
*DIP ALU WR → DOP	Ic	LLLL – HHHH	HH	LLL
*DIP ALU WR → WR	Id	LLLL – HHHH	HH	LLH
DIP ALU WR → XWR	If	LLLL – HHHH	HH	HLL
DIP ALU XWR → DOP	Ih	LLLL – HHHH	HH	HHH
DIP ALU XWR → WR	Ie	LLLL – HHHH	HH	LHH
DIP ALU XWR → XWR	Ig	LLLL – HHHH	HH	HHL
(DIP plus WR plus ALUCIN) LCIR → WR, XWR	IVb	HLLH	HH	LHL
(DIP plus WR plus ALUCIN) RSA → WR, XWR	IVa	HLHH	HH	LHL
DIP plus RF plus ALUCIN → RF	IId	LHHH	HL	LLL – HHH
DIP plus RF plus ALUCIN → WR	IIb	LHLL	HL	LLL – HHH
DIP plus RF plus ALUCIN → XWR	IIc	LHLH	HL	LLL – HHH
DIP plus WR plus ALUCIN → DOP	IIi,IIIh	LHHH	HH	LHL
DIP plus WR plus ALUCIN → XWR	IIh	LLHH	HH	LHL
DIP plus XWR plus ALUCIN → WR	IIj	HHLL	HH	LHL
DIP plus XWR plus ALUCIN → XWR	IIk	HHLH	HH	LHL

*XWR → AOP, otherwise WR → AOP. PC PRIORITY = HIGH overrides.

TABLE 34
RF SOURCE OPERANDS

OPERATION	OP FORM/TYPE	OP3 · OP0 OP FIELD	D1 D0 D-FIELD	S2 · S0 S-FIELD
RF → DOP	IIIb	LLLL	HL	LLL · HHH
RF → XWR	IIIc	LLLH	HL	LLL → HHH
RF ALU WR → RF	Ia	LLLL · HHHH	LL	LLL · HHH
RF ALU WR → WR	Ib	LLLL · HHHH	LH	LLL → HHH
RF plus DIP plus ALUCIN → RF	IId	LHHH	HL	LLL · HHH
RF plus DIP plus ALUCIN → WR	IIb	LHLL	HL	LLL → HHH
RF plus DIP plus ALUCIN · XWR	IIc	LHLH	HL	LLL → HHH
(RF plus WR plus ALUCIN, XWR) LCIR → WR, XWR	IVd	HLLH	HL	LLL → HHH
(RF plus WR plus ALUCIN, XWR) RSA · WR, XWR	IVi	HLHH	HL	LLL → HHH
RF plus WR plus ALUCIN → XWR	IIa	LLHH	HL	LLL · HHH
RF plus XWR plus ALUCIN → WR	IIe	HHLL	HL	LLL · HHH
RF plus XWR plus ALUCIN → XWR	IIf	HHLH	HL	LLL · HHH

NOTE: When PC PRIORITY is LOW, WR · AOP.

TABLE 35
XWR SOURCE OPERANDS

OPERATION	OP FORM/TYPE	OP3 → OP0 OP FIELD	D1 D0 D-FIELD	S2 → S0 S-FIELD
XWR ALU DIP → DOP	Ih	LLLL → HHHH	HH	HHH
XWR ALU DIP → WR	Ie	LLLL → HHHH	HH	LHH
XWR ALU DIP → XWR	Ig	LLLL → HHHH	HH	HHL
XWR plus ALUCIN → DOP	III	HHHL	HH	LHL
XWR plus ALUCIN → RF	IIj	HHHL	HL	LLL · HHH
XWR plus DIP plus ALUCIN → WR	IIk	HHLL	HH	LHL
XWR plus DIP plus ALUCIN → XWR	IIe	HHLH	HH	LHL
XWR plus RF plus ALUCIN → WR	IIf	HHLL	HL	LLL → HHH
XWR plus RF plus ALUCIN → XWR		HHLH	HL	LLL → HHH

NOTE: When PC PRIORITY is LOW, WR → AOP.

TABLE 36
WR SOURCE OPERANDS

OPERATION	OP FORM/TYPE	OP3 → OP0 OP-FIELD	D1 D0 D-FIELD	S2 → S0 S-FIELD
*WR ALU DIP → DOP	Ic	LLLL → HHHH	HH	LLL
*WR ALU DIP → WR	Id	LLLL → HHHH	HH	LLH
WR ALU DIP → XWR	If	LLLL → HHHH	HH	HLL
WR ALU RF → RF	Ia	LLLL → HHHH	LL	LLL → HHH
WR ALU RF → WR	Ib	LLLL → HHHH	LH	LLL → HHH
(WR minus BIP minus 1 plus ALUCIN, XWR) LCIR → WR, XWR	IVa	HLLL	HH	LHL
(WR minus DIP minus 1 plus ALUCIN, XWR) RSA → WR, XWR	IVf	LLHL	HH	LHL
(WR minus RF minus 1 plus ALUCIN, XWR) LCIR → WR, XWR	IVc	HLLL	HL	LLL → HHH
(WR minus RF minus 1 plus ALUCIN, XWR) RSA → WR, XWR	IVh	LLHL	HL	LLL → HHH
(WR plus ALUCIN) RSA → WR, XWR	IVe	HLHL	HL	XXX
(WR plus ALUCIN) RSA → WR, XWR	IVe	HLHL	HH	LHL
(WR plus ALUCIN) LCIR → WR	Vd	LLHH	HH	HLH
(WR plus ALUCIN) LCIR → WR	Vd	HLHH	HH	HLH
(WR plus ALUCIN) LSA → WR	Vc	LLHL	HH	HLH
(WR plus ALUCIN) LSL → WR	Vf	HLHL	HH	HLH
(WR plus ALUCIN) RCIR → WR	Vb	LLLH	HH	HLH
(WR plus ALUCIN) RCIR → WR	Vb	HLLH	HH	HLH
(WR plus ALUCIN) RSA → WR	Va	LLLL	HH	HLH
(WR plus ALUCIN) RSL → WR	Ve	HLLL	HH	HLH
(WR plus ALUCIN, XWR) LCIR → (WR, XWR)	VId	HHHH	HH	HLH
(WR plus ALUCIN, XWR) LCIR → (WR, XWR)	VId	LHHH	HH	HLH
(WR plus ALUCIN, XWR) LSA → (WR,XWR)	VIc	LHHL	HH	HLH
(WR plus ALUCIN, XWR) LSL → (WR, XWR)	VIf	HHHL	HH	HLH
(WR plus ALUCIN, XWR) RCIR → (WR, XWR)	VIb	HHLH	HH	HLH
(WR plus ALUCIN, XWR) RCIR → (WR, XWR)	VIb	LHLH	HH	HLH
(WR plus ALUCIN, XWR) RSA → (WR, XWR)	VIa	LHLL	HH	HLH
(WR plus ALUCIN, XWR) RSL → (WR,XWR)	VIe	HHLL	HH	HLH
WR plus DIP plus ALUCIN → DOP	IIi	LHHH	HH	LHL
WR plus DIP plus ALUCIN → XWR	IIh	LLHH	HH	LHL
(WR plus DIP plus ALUCIN) LCIR → WR, XWR	IVb	HLLH	HH	LHL
(WR plus DIP plus ALUCIN) RSA → WR, XWR	IVc	HLHH	HH	LHL
WR plus RF plus ALUCIN → XWR	IIa	LLHH	HL	LLL HHH
(WR plus RF plus ALUCIN) LCIR → WR, XWR	IVd	HLLH	HL	LLL HHH
(WR plus RF plus ALUCIN) RSA → WR, XWR	IVi	HLHH	HL	LLL HHH

*XWR → AOP, otherwise WR → AOP. PC PRIORITY = HIGH overrides.

6. INTERFACING

The input/output (I/O) accommodations of these processor elements have been designed for TTL and/or MOS compatibility. Direct interfacing, supportable by the entire families of catalog devices, is shown in Figure 22. Typical data/address flow and microcontrol are illustrated for an expanded wordlength system.

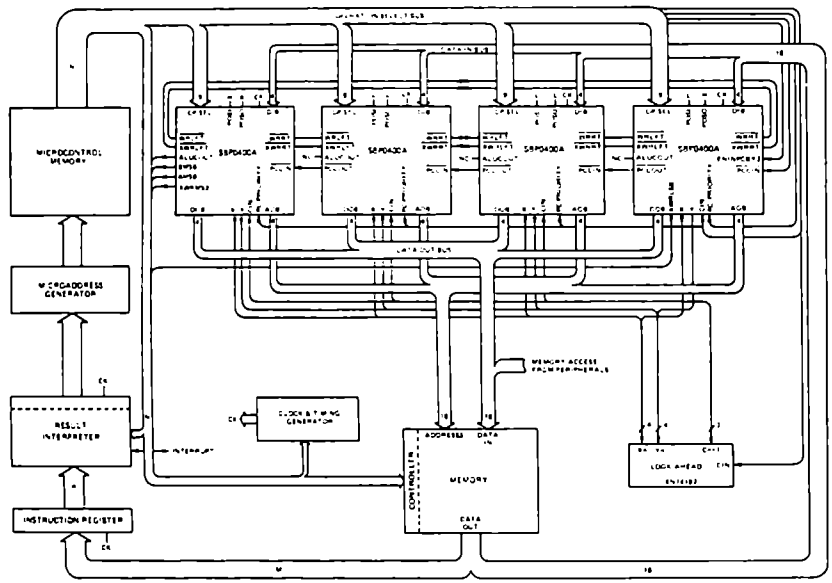


FIGURE 22 – TYPICAL 16-BIT MACHINE

6.1 INPUT CIRCUIT

The input circuit used on the '0400A/'0401A is basically an RTL configuration which has been modified for TTL/MOS compatibility as shown in Figure 23A. An input-clamping diode is incorporated to limit negative excursions (ringing) when the '0400A/'0401A is on the receiving end of a transmission line; an input switching threshold of nominally +1.5 volts has been specified for improved noise immunity. This threshold is achieved via two 10K ohm resistors which function as a voltage divider to increase the one V_{BE} threshold of the I^2L input transistor to +1.5 volts. Since this input circuit is independent of injector current, input threshold compatibility is maintained over the entire speed X power performance spectrum.

The input circuit characteristics for input current versus input voltage are shown in Figure 24. The 10K and 20K ohm load lines and threshold knee at +1.5 volts provide a high-impedance characteristic to reduce input loading and improve the low-logic level input noise immunity over some standard TTL inputs. Full compatibility is maintained with virtually all 5 volt logic families even when the '0400A/'0401A is powered down (injector current reduced).

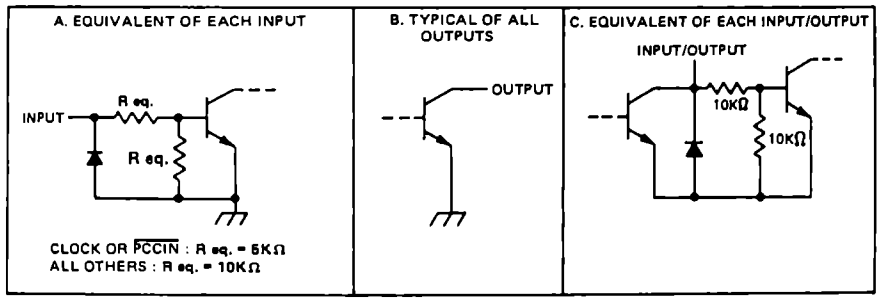


FIGURE 23 – SCHEMATICS OF EQUIVALENT INPUTS, OUTPUTS, INPUTS/OUTPUTS

6.1.1 Sourcing Inputs

The inputs may be sourced directly by most 5 volt logic families. Five volt functions which feature internal pull-up resistors at their outputs require no external interface components; five volt functions which feature open-collector outputs generally require external pull-up resistors which may be specified as shown in Table 37.

6.1.2 Terminating Unused Inputs

Inputs which are selected to be hardwired to a logic-level low may be connected directly to ground. Inputs which are selected to be hardwired to a logic-level high must be tied, via a current limiting (pull-up) resistor, to a logic-level-high low-impedance voltage source such as V_{CC}. A single transient protecting resistor, specified as shown in Table 38, may be utilized common to (N) inputs.

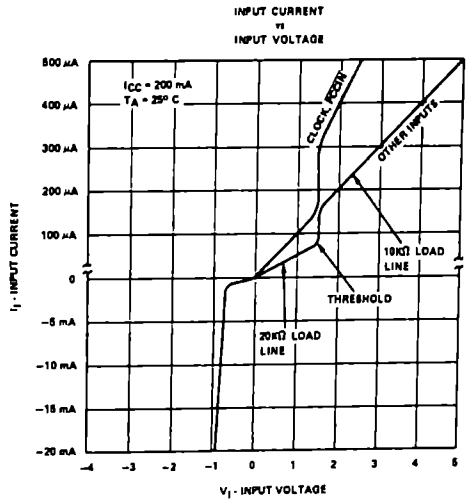


FIGURE 24 – TYPICAL INPUT CHARACTERISTICS

6.2 OUTPUT CIRCUIT

The output circuit selected for the '0400A/'0401A is an injected open-collector transistor shown in Figure 23B. Since this transistor is injected, output sourcing capability is directly related to injector current. In other words, the number of loads which may be sourced by an '0400A/'0401A output is directly reduced as injector current is reduced.

The output circuit characteristic for logic-level low output voltage (V_{OL}) versus logic-level low output current (I_{OL}) is shown in Figure 25. At rated injector current, the '0400A/'0401A output circuit offers a low-level output voltage of typically 65mV.

TABLE 37
SOURCING SBP0400 INPUTS

	CLOCK OR $\overline{PCCIN}$	ALL OTHER INPUTS
SOURCED BY OPEN-COLLECTOR TTL, CMOS	$R_P = \frac{V_{CC} - 3.3}{.0005\ (N)}$	$R_P = \frac{V_{CC} - 3.3}{.00025\ (N)}$
SOURCED BY MOS, CMOS: LOW-THRESHOLD	$R_B = \frac{V_{CC} - 2.4}{I_{OH} - .0005\ (N)}$	$R_B = \frac{V_{CC} - 2.4}{I_{OH} - .00025\ (N)}$
HIGH-THRESHOLD	NOT RECOMMENDED	
SOURCED BY TTL WITH 5 V ACTIVE PULL-UP	DRIVE DIRECTLY	

TABLE 38
TERMINATING UNUSED INPUTS

	$\overline{PCCIN}$ INPUT	ALL OTHER INPUTS
HARDWIRE TO V_{IH}	$R_P = \frac{V_{CC} - 3.3}{.0005\ (N)}$	$R_P = \frac{V_{CC} - 3.3}{.00025\ (N)}$

The output circuit characteristics for 1) logic-level high output voltage (V_{OH}) and current (I_{OH}), 2) rise times, and 3) next stage input noise immunity, are a function of the load circuit being sourced. The load circuit may be either:

A) the direct input, if no source current is required, of a five-volt logic family function,

or, for greater noise immunity and improved rise times,

B) the direct input of a five-volt logic family function in conjunction with a discrete pull-up resistor.

When a discrete pull-up resistor (R_L) is utilized, the fanout requirements placed on a particular '0400A/'0401A output restrict both the maximum and minimum value of R_L. Techniques for calculating $R_{L(max)}$ and $R_{L(min)}$ respectively are explained in Figure 26. Table 39 provides $R_{L(max)}$ and $R_{L(min)}$ values for one, five, nine, or ten loads for the more popular five-volt logic families.

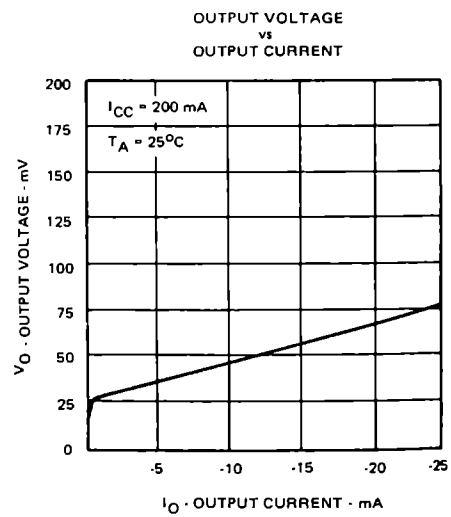


FIGURE 25 – TYPICAL OUTPUT CHARACTERISTICS

6.2.1 $R_{L(max)}$ Calculation for Output Source Current

The maximum load register $R_{L(max)}$ value insures: 1) that sufficient current is available to satisfy both the fanout and logic-level-high output current requirements, and 2) that the voltage drop across R_L itself is insufficient to reduce the logic-level-high output voltage below 2.4 volts. $R_{L(max)}$ can be calculated as shown in Figure 26A.

HIGH-LEVEL (OFF-STATE) CIRCUIT CALCULATIONS

The allowable voltage drop across the load resistor (V_{RL}) is the difference between the pull-up source and the V_{OH} level required at the load:

$$V_{RL} = V_{source} - V_{OH\ min}$$

The total current through the load resistor (I_{RL}) is the sum of the load current and the high-level output current (I_{OH}):

I_{RL} = Load Current (into the load inputs + I_{OH}

where I_{OH} = 375 μA max

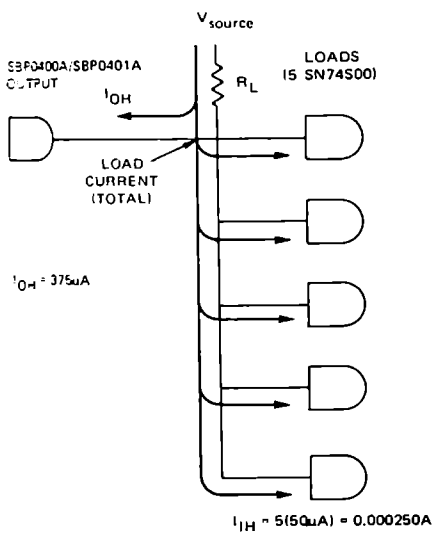
Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} \text{ in ohms} = \frac{V_{source} - V_{OH\ min}}{\text{Amperes of Load Current} + .000375}$$

LOW-LEVEL (ON-STATE) CIRCUIT CALCULATIONS

The maximum current through the load resistor when the output is on, plus the amount of current from the low-level input load, must be limited to the I_{OL} capability of the output. Therefore, the equation is:

$$R_{L(min)} = \frac{V_{source} - V_{OL\ max}}{I_{OL\ capability} - I_{load}}$$



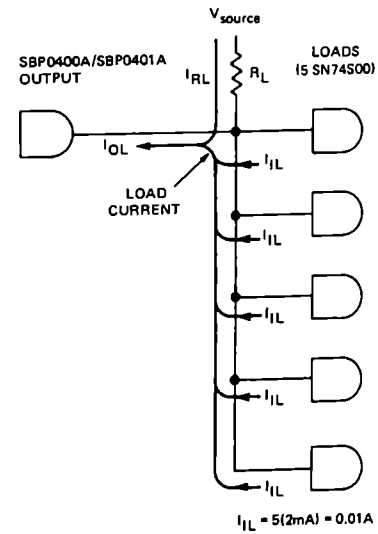
I_{IH} = 5(50uA) = 0.000250A

Assume: V_{source} = 5 V and $V_{OH(min)}$ = 2.4 V

$$R_{L(max)} = \frac{V_{source} - V_{OH}}{I_{load} + 0.000375}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.00025 + 0.000375}\ \Omega = \frac{2.6}{0.000625}\ \Omega = 4160$$

A. R_L MAXIMUM CALCULATIONS



I_{IL} = 5(2mA) = 0.01A

Assume: V_{source} = 5 V, V_{OL} = 0.4 V, and I_{OL} capability = 20 mA

$$R_{L(min)} = \frac{V_{source} - V_{OL}}{I_{OL\ capability} - I_{IL}}$$

$$R_{L(min)} = \frac{5 - .4}{0.02 - 0.01}\ \Omega = \frac{4.6}{0.01}\ \Omega = 460\ \Omega$$

B. R_L MINIMUM CALMCLATIONS

FIGURE 26 – OUTPUT LOAD RESISTOR CALCULATIONS

TABLE 39
OUTPUT LOAD RESISTOR VALUES (R_L)

SBP0400 OUTPUT TYPE	DRIVING 1 Load		DRIVING 5 Loads		DRIVING 10 Loads		TYPE OF LOGIC
	RL(MIN)	RL(MAX)	RL(MIN)	RL(MAX)	RL(MIN)	RL(MAX)	
	234 Ω	6190 Ω	252 Ω	5200 Ω	280 Ω	4333 Ω	54LS/74LS
20 mA	250 Ω	5909 Ω	383 Ω	4333 Ω	1150 Ω	3250 Ω	54/74
SINK	256 Ω	5777 Ω	460 Ω	4160 Ω	2300 Ω	2888 Ω	54S/74S
OUTPUTS	230 Ω	6341 Ω	230 Ω	5777 Ω	231 Ω	5200 Ω	MOS
	230 Ω	6500 Ω	230 Ω	6500 Ω	231 Ω	6498 Ω	C-MOS
	477 Ω	6190 Ω	560 Ω	5200 Ω	TYPE OF LOGIC		
10 mA	547 Ω	5909 Ω	2300 Ω	4333 Ω	54LS/74LS		
SINK	575 Ω	5777 Ω	4000 Ω	4000 Ω	54/74		
OUTPUTS	464 Ω	6341 Ω	462 Ω	5777 Ω	54S/74S		
	460 Ω	6500 Ω	460 Ω	6500 Ω	MOS		
					C-MOS		

Specific designs can be tailored for minimum power or maximum performance by making the individual calculations as described in Figure 26.

CONDITIONS:

V_{source} = 5 V
V_{OH} = 2.4 V (Satisfies most 5 V logic)
V_{OL} = 0.4 V (Based on max noise margin provided by SBP0400A/SBP0401A
I_{OH} = 375 μA (Maximum leakage of SBP0400A/SBP0401A)
I_{OL} as specified (20 mA, 10 mA)

And unit loads of:	I_{IL} =	I_{IH} =
54LS/74LS	0.36 mA	10 μA
54/74	1.6 mA	40 μA
54S/74S	2 mA	50 μA
N-MOS	10 μA	10 μA
C-MOS	10 pA	10 pA

6.2.2 $R_{L(min)}$ Calculation for Output Source Current

The minimum load resistor $R_{L(min)}$ value insures that the arithmetic sum of the current through R_L itself plus the sink currents from the various loads will not exceed the low-level current rating (I_{OL}) of the particular output being utilized. $R_{L(min)}$ may be calculated as shown in Figure 26B.

6.3 BIDIRECTIONAL INPUT/OUTPUT CIRCUIT

The bidirectional input/output circuit, shown in Figure 23C, is simply a "marriage" of the separate input and output circuits, with the respective electrical characteristics described above.

7. POWER SOURCE

I^2L is a current-injected logic. When placed across a curve tracer, the processor element will resemble a silicon switching diode. Any voltage or current source capable of supplying the desired current at the injector node voltage

required will suffice (see Table 40). A dry-cell battery, a 5-volt TTL power supply, a programmable current supply (for power-up/power-down operation) — literally whatever power source is convenient can be used for most cases. For example, if a 5-volt TTL power supply is to be used, a series dropping resistor would be connected between the 5-volt supply and the injector pins of the I^2L device, as illustrated in Figure 27, to select the desired operating current. In expanded systems using multiple 4 bit slices, an individual dropping resistor is required for each SBP0400A/SBP0401A.

Figures 28 and 29 show the typical injector node voltages which occur across the temperature and injector current ranges. Table 40 provides the approximate resistor values for various combinations of supply voltages and operating injector currents.

TABLE 40
INJECTOR CURRENT LIMITING RESISTOR VALUES

Injector Current	0.01 mA	0.1 mA	1 mA	10 mA	100 mA	200 mA	Supply Voltage
RESISTOR VALUE (OHMS)	1.1M	114K	11K	1.1K	110	56	12V
	840K	84K	8.4K	830	82	41	9V
	540K	54K	5.4K	530	52	26	6V
	440K	44K	4.4K	430	42	21	5V
	390K	39K	3.9K	380	37	18	4.5V
	240K	24K	2.4K	230	22	11	3V
	90K	9K	960	82	7	3.25	1.5V
	63K	6K	550	50	4	1.75	1.2V

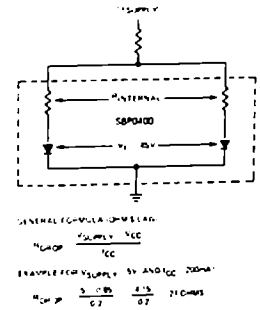


FIGURE 27 – INJECTOR CURRENT CALCULATIONS

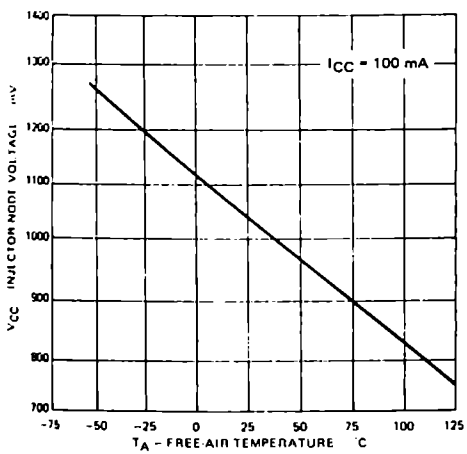


FIGURE 28 – INJECTOR-NODE VOLTAGE VS. FREE-AIR TEMPERATURE

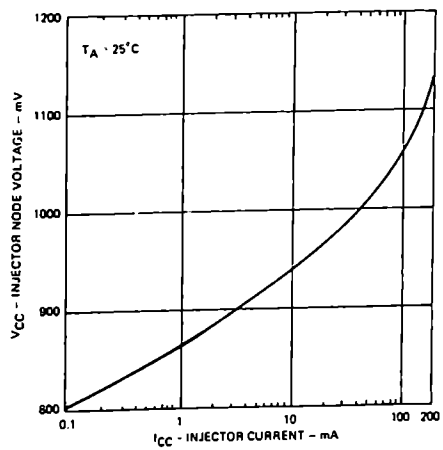


FIGURE 29 – INJECTOR-NODE VOLTAGE VS. INJECTOR CURRENT

8. ELECTRICAL AND MECHANICAL SPECIFICATIONS

8.1 RECOMMENDED OPERATING CONDITIONS, UNLESS OTHERWISE NOTED I_{CC} = 200 mA

		SBP0400AM			SBP0400AC			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply current, I_{CC}			200	300		200	300	mA
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}	Any AOP, X, Y, ALUCOUT, DOP, or XWR MSB/LSB			20			20	mA
	$\overline{XWRLFT}$, $\overline{XWRRT}$, $\overline{WRRT}$, $\overline{WRLFT}$, $\overline{PCCOUT}$/BMSB, ENINCBY 2/AMSB			10			10	
Width of clock pulse, t_w	High		255			230		ns
	Low		50			45		
Setup time, t_{su} (See Figure 30)	OPERATION SELECT (0400A ONLY)		78			70		ns
	$\overline{PCCIN}$		28			25		
	DIP → RF, WR, XWR		110			100		
	DIP THRU ALU		200			180		
	ALUCIN		132			120		
Hold time, t_h (any input)			0†			0†		ns
Operating free-air temperature, T_A		−55		125	0		70	C

† Rising edge of clock pulse is reference

8.2 ELECTRICAL CHARACTERISTICS (OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE, UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS†	SBP0400AM			SBP0400AC			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		I_{CC} = 200 mA, I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High-level output current		I_{CC} = 200 mA, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V			400			250	μA
V_{OL}	Low-level output voltage		I_{CC} = 200 mA, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.4			0.4	V
I_I	Input current	Clock, $\overline{PCCIN}$	I_{CC} = 200 mA, V_I = 2.5 V			500			500	μA
		All other inputs				250			250	

† For conditions shown as MAX, use the appropriate value specified under recommended operating conditions
‡ All typical values are at I_{CC} = 200 mA, T_A = 25°C.

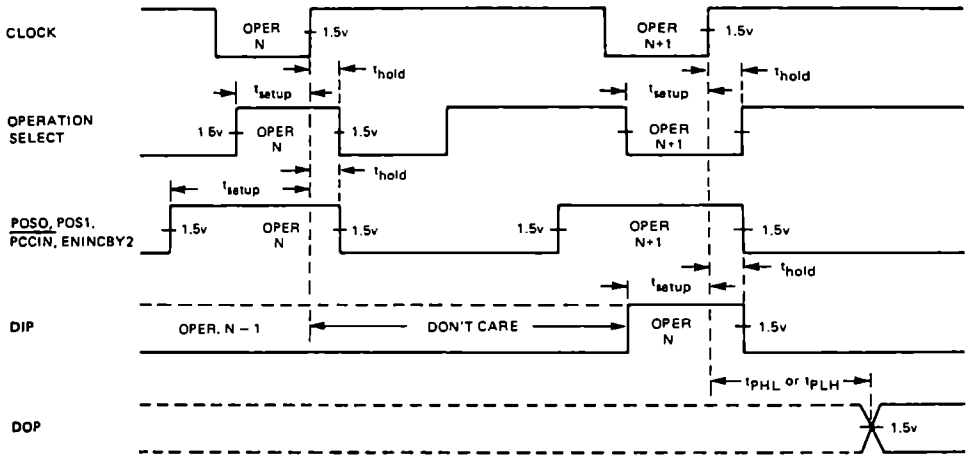
TENTATIVE DATA SHEET
This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

8.3 SBP0400A AND SBP0401A SWITCHING CHARACTERISTICS (I_{CC} = 200 mA, T_A = 25°C) SEE FIGURES 30 THROUGH 34

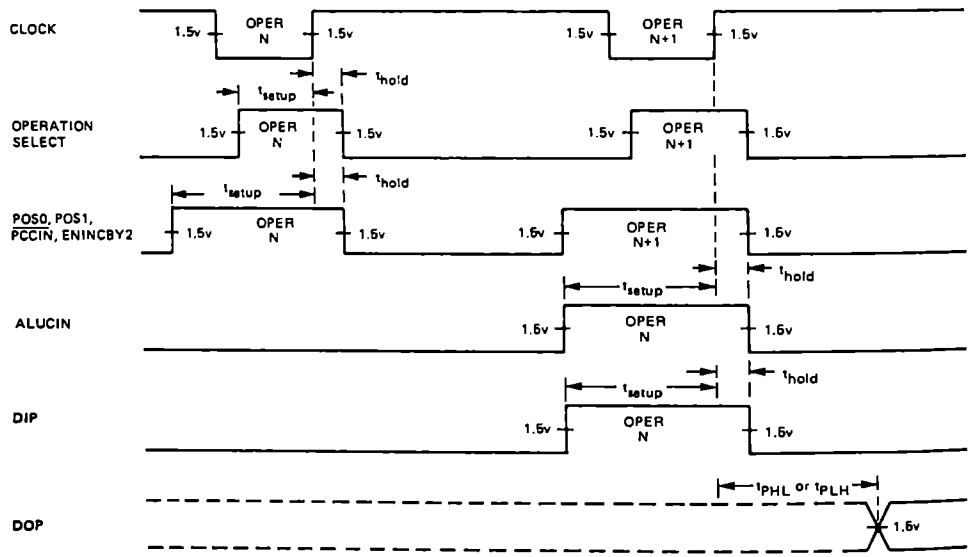
PARAMETER	FROM	TO	TEST CONDITIONS	TYP	MAX	UNIT
t_{PLH} or t_{PHL}	DIP	DOP	VIA A BUS, BYPASS ALU	85		ns
t_{PLH} or t_{PHL}	DIP	DOP	VIA A BUS, THRU ALU	155		ns
t_{PLH} or t_{PHL}	DIP	DOP	VIA B BUS, THRU ALU	155		ns
t_{PLH} or t_{PHL}	PC PRIORITY	AOP		70		ns
t_{PLH} or t_{PHL}	ALUCIN	ALUCOUT		60		ns
t_{PLH} or t_{PHL}	DIP	ENINCBY2/AMSB	POS0 = X, POS1 = H	80		ns
t_{PLH} or t_{PHL}	DIP	$\overline{PCCOUT}$/BMSB	POS0 = X, POS1 = H	80		ns
t_{PLH} or t_{PHL}	POS0, or POS1	ENINCBY2/AMSB or $\overline{PCCOUT}$/BMSB		95		ns
t_{PLH} or t_{PHL}	$\overline{PCCIN}$	$\overline{PCCOUT}$		35		ns
t_{PLH} or t_{PHL}	ALUCIN	DOP		105		ns
t_{PLH} or t_{PHL}	CLOCK	$\overline{PCCOUT}$/BMSB	POS0 = X, POS1 = H	140		ns
t_{PLH} or t_{PHL}	CLOCK	DOP	VIA A BUS, BYPASS ALU	155		ns
t_{PLH} or t_{PHL}	CLOCK	DOP	VIA A BUS, THRU ALU	240		ns
t_{PLH} or t_{PHL}	CLOCK	ENINCBY2/AMSB	POS0 = X, POS1 = H	155		ns
t_{PLH} or t_{PHL}	CLOCK	DOP	VIA B BUS, THRU ALU	225		ns
t_{PLH} or t_{PHL}	CLOCK	$\overline{P}$, $\overline{G}$, or ALUCOUT	VIA A OR B BUS, THRU ALU	180		ns
t_{PLH} or t_{PHL}	CLOCK	AOP		105		ns
t_{PLH} or t_{PHL}	CLOCK	$\overline{WRLFT}$, $\overline{WRRT}$, $\overline{XWRLFT}$, or $\overline{XWRRT}$		240		ns
t_{PLH} or t_{PHL}	CLOCK	XWR MUX MSB	POS0 = H, POS1 = H	130		ns
t_{PLH} or t_{PHL}	CLOCK	XWR MUX LSB	POS0 = H, POS1 = L	130		ns
t_{PLH} or t_{PHL}	CLOCK	ALU = 0		215		ns

8.4 SBP0401A OPERATION SELECT SWITCHING CHARACTERISTICS (I_{CC} = 200 mA, T_A = 25 °C) SEE FIGURES 31 THROUGH 34

PARAMETER	FROM	TO	TEST CONDITIONS	TYP	MAX	UNIT
t_{PLH} or t_{PHL}	OP SEL	XWR MUX MSB	POS0 = H, POS1 = H	175		ns
t_{PLH} or t_{PHL}	OP SEL	XWR MUX LSB	POS0 = H, POS1 = L	175		ns
t_{PLH} or t_{PHL}	OP SEL	AOP		130		ns
t_{PLH} or t_{PHL}	OP SEL	ALU = 0		215		ns
t_{PLH} or t_{PHL}	OP SEL	$\overline{P}$, $\overline{G}$, or ALUCOUT	Via A or B bus, thru ALU	180		ns
t_{PLH} or t_{PHL}	OP SEL	DOP	Via A or B bus, thru ALU	235		ns
t_{PLH} or t_{PHL}	OP SEL	AMSB	POS0 = X, POS1 = H	140		ns
t_{PLH} or t_{PHL}	OP SEL	BMSB	POS0 = X, POS1 = H	175		ns



SETUP, HOLD, AND PROPAGATION DELAY TIMES FOR TYPICAL SBP0400A STORE OPERATION



SETUP, HOLD, AND PROPAGATION DELAY TIMES FOR TYPICAL SBP0400A ADD AND SHIFT OPERATION

FIGURE 30 – PROPAGATION DELAY TIMES – SBP0400A SYNCHRONOUS OPERATIONS

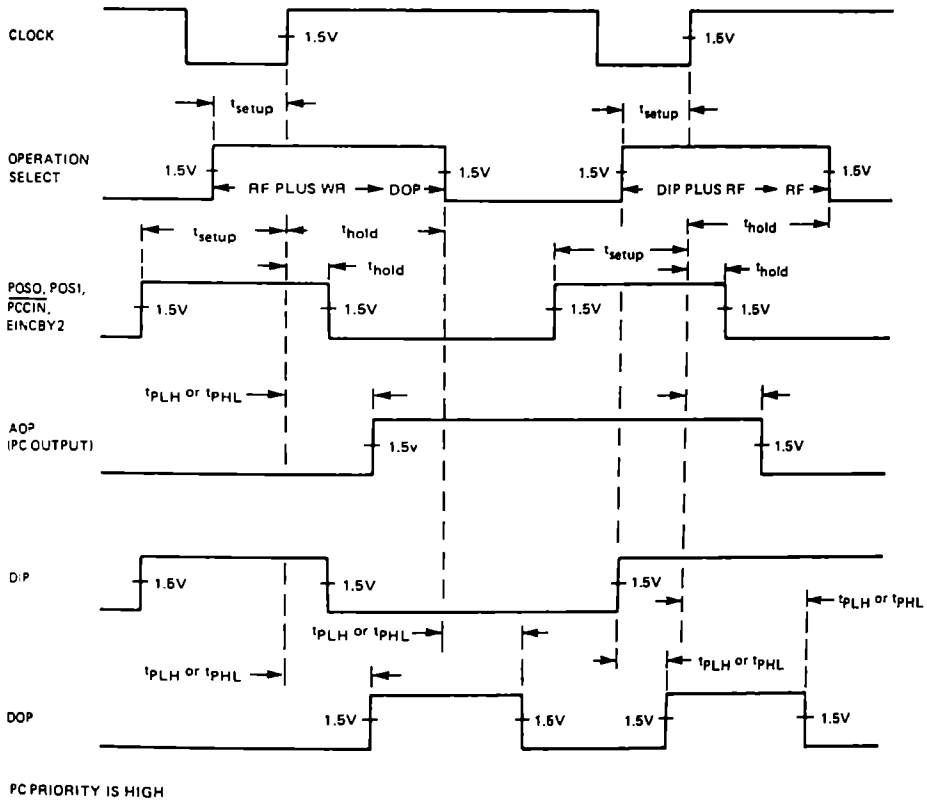


FIGURE 31 – PROPAGATION DELAY TIMES – ASYNCHRONOUS OPERATIONS

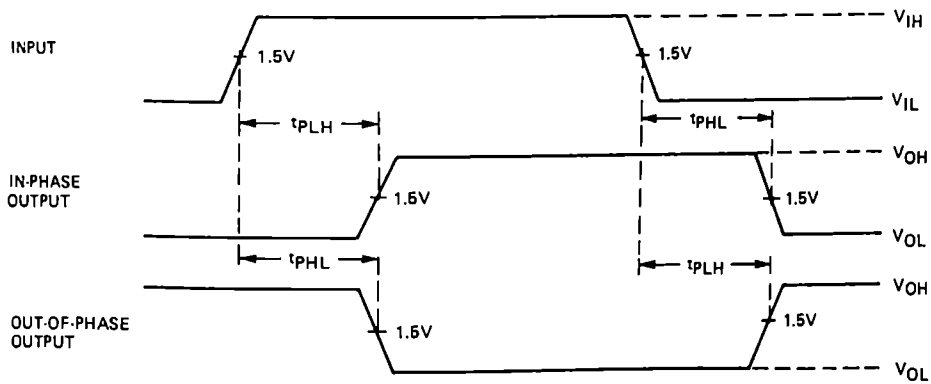
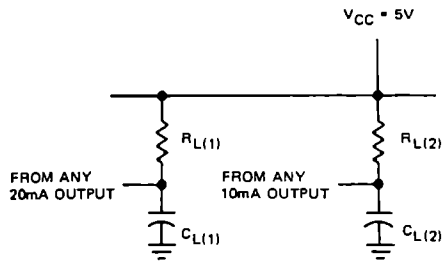
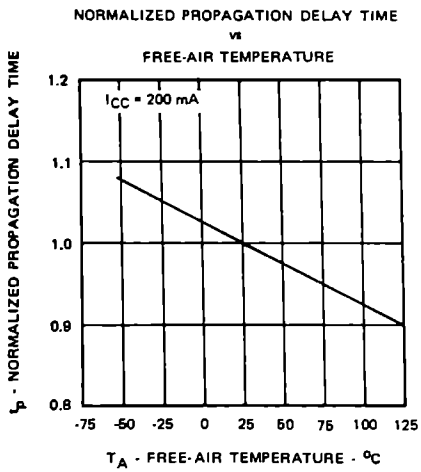


FIGURE 32 – PROPAGATION DELAY TIMES – ASYNCHRONOUS OPERATIONS



REF.	OUTPUTS	MAXIMUM CURRENT RATING	R_L VALUE	C_L VALUE
1	ANY AOB, DOB, $\overline{P}$, $\overline{G}$, ALUCOUT OR XWR MSB/LSB	20 mA	280 Ω	50 pF
2	$\overline{XWRLFT}$, $\overline{XWRRT}$, $\overline{WRRT}$, $\overline{WRLFT}$, $\overline{PCCOUT}$/BMSB, ENINCBY2/AMSB	10 mA	560 Ω	25 pF

FIGURE 33 – SWITCHING TIMES LOAD CIRCUITS



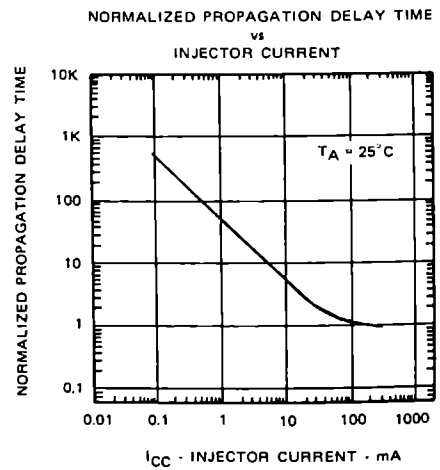


FIGURE 34 – TYPICAL SWITCHING CHARACTERISTICS

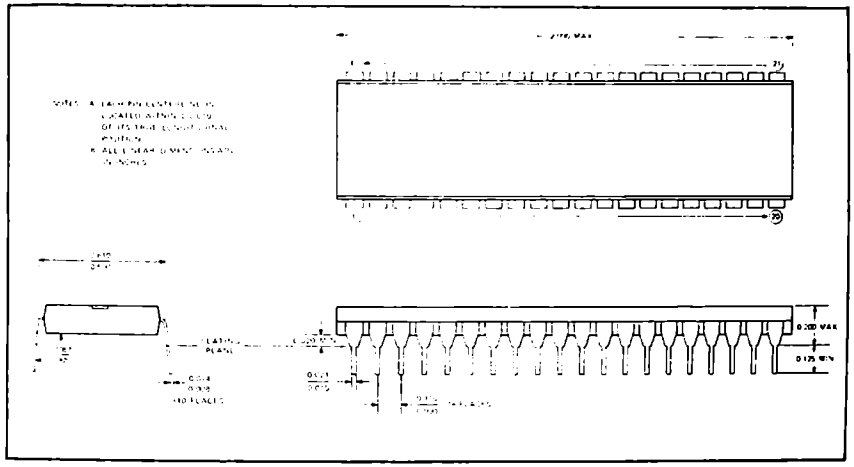


FIGURE 35 – PLASTIC DUAL-IN-LINE PACKAGE

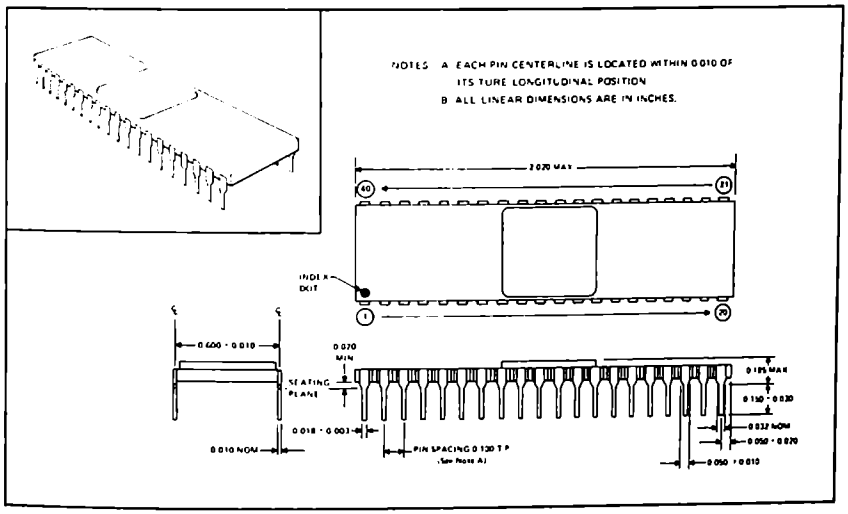


FIGURE 36 – CERAMIC DUAL-IN-LINE PACKAGE

8.5 ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE	PART NUMBERS
PLASTIC DIP	0°C to 70°C	SBP0400ACN or SBP0401ACN
CERAMIC DIP	0°C to 70°C	SBP0400ACJ or SBP0401ACJ
	–55°C to 125°C	SBP0400AMJ or SBP0401AMJ

The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

SBP 9900
I^2L 16-Bit Microprocessor Data Manual

OCTOBER 1976

TEXAS INSTRUMENTS
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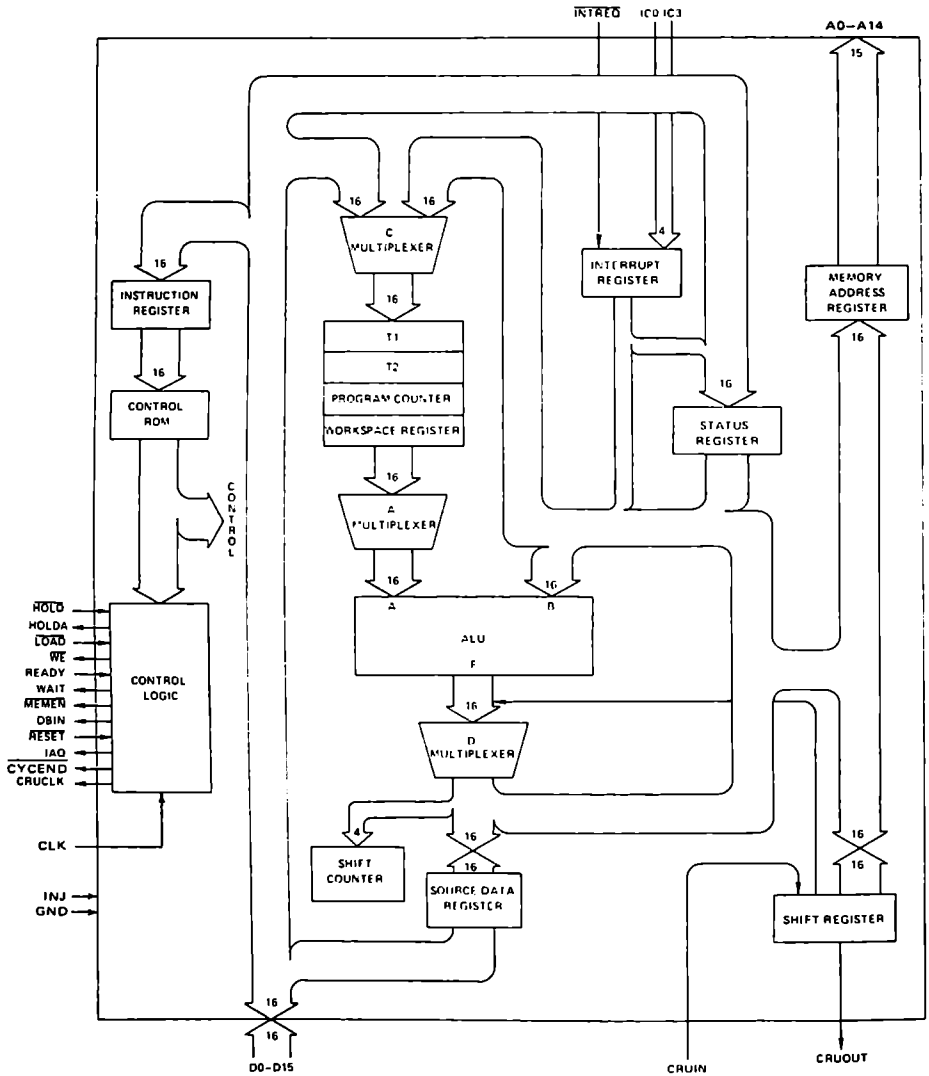


FIGURE 1 – SBP 9900 ARCHITECTURE

1. INTRODUCTION

1.1 DESCRIPTION

The SBP 9900 microprocessor is a ruggedized monolithic parallel 16-bit Central Processing Unit (CPU) fabricated with Integrated Injection Logic (I^2L) technology. The SBP 9900 combines the properties of I^2L technology with a 16-bit word length, an advanced memory to memory architecture, and a full minicomputer instruction set to extend the end application reach of Texas Instruments 9900 microprocessor family into those applications requiring efficient, stable, reliable performance in severe operating environments. I^2L technology enables the SBP9900 to operate over a −55 to 125°C ambient temperature range from a single d-c power source with user selectable speed/power performance. Static Logic is used throughout with directly TTL compatible I/O permitting use with standard logic and memory devices and thereby eliminating the need for special clock and interface functions. The SBP 9900 is software compatible with other 9900 microprocessor family members and shares a common body of hardware/software with Texas Instruments 990 minicomputer family.

1.2 KEY FEATURES

- Parallel 16-Bit Word Length
- Full Minicomputer Instruction Set Includes Multiply and Divide
- Directly Addresses Up to 65,536 Bytes/32,768 Words of Memory
- Advanced Memory-To-Memory Architecture
- Multiple 16-Word Register Files (Work Spaces) Reside in Memory
- Separate I/O, Memory and Interrupt Bus Structures
- 16 Prioritized Hardware Interrupts
- 16 Software Interrupts (XOPS)
- Programmed and DMA I/O Capability
- Serial I/O Via Communications-Register-Unit (CRU)
- 64-Pin Package
- Software Compatible with TI 9900 Microprocessor/990 Minicomputer Family
- I^2L Technology:
  - −55°C to 125°C Ambient Temperature Range
  - User Selectable Speed/Power Operation
  - 2.6 MHz Nominal Clock at 500 mW
  - Single d-c Power Supply
  - Fully Static Operation
  - Single Phase Clock
  - Directly TTL Compatible I/O (Including Clock)

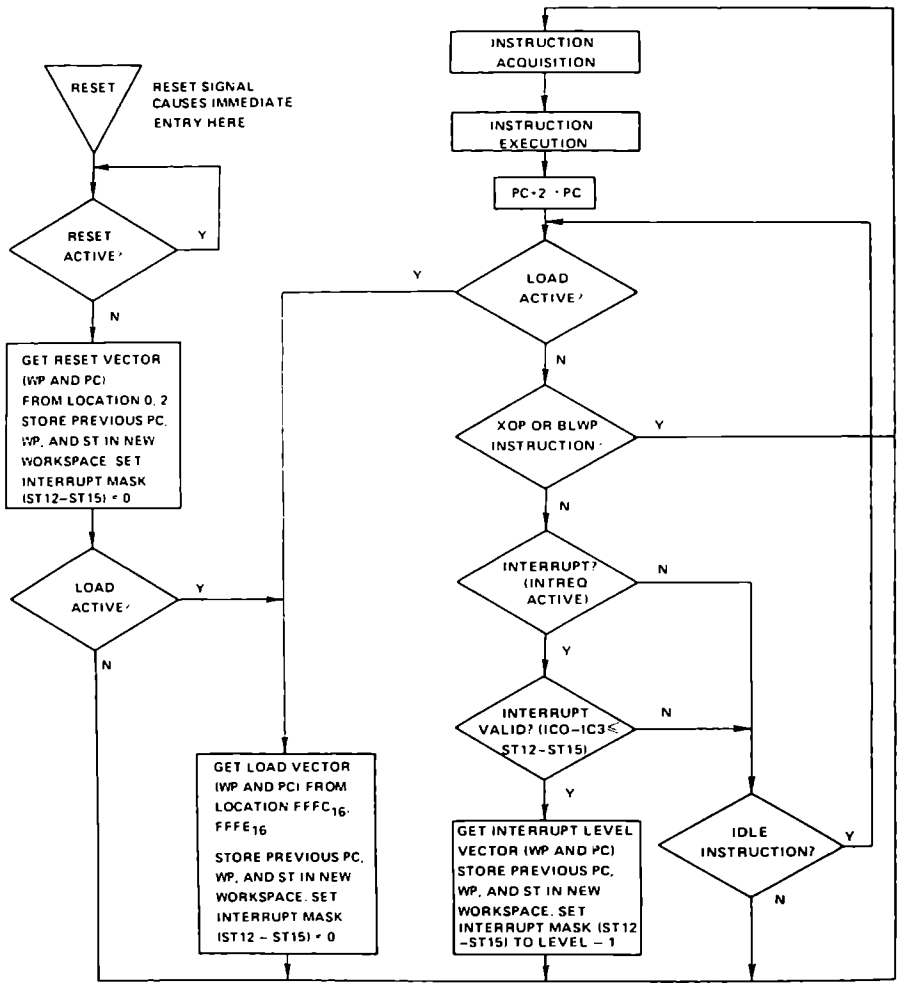

RESET
RESET SIGNAL CAUSES IMMEDIATE ENTRY HERE
RESET ACTIVE?
Y
N
GET RESET VECTOR (WP AND PC) FROM LOCATION 0, 2 STORE PREVIOUS PC, WP, AND ST IN NEW WORKSPACE SET INTERRUPT MASK (ST12–ST15) = 0
LOAD ACTIVE?
Y
N
GET LOAD VECTOR (WP AND PC) FROM LOCATION FFFC16, FFFE16
STORE PREVIOUS PC, WP, AND ST IN NEW WORKSPACE. SET INTERRUPT MASK (ST12 – ST15) = 0
INSTRUCTION ACQUISITION
INSTRUCTION EXECUTION
PC←2 + PC
LOAD ACTIVE?
Y
N
XOP OR BLWP INSTRUCTION?
Y
N
INTERRUPT? (INTREQ ACTIVE)
N
Y
INTERRUPT VALID? (IC0–IC3 ≤ ST12–ST15)
N
Y
GET INTERRUPT LEVEL VECTOR (WP AND PC) STORE PREVIOUS PC, WP, AND ST IN NEW WORKSPACE. SET INTERRUPT MASK (ST12 –ST15) TO LEVEL – 1
IDLE INSTRUCTION?
Y
N

FIGURE 2 – 9900 CPU FLOW CHART

2. ARCHITECTURE

The memory word of the 9900 is 16 bits long. Each word is also defined as 2 bytes of 8 bits. The instruction set of the 9900 allows both word and byte operands. Thus, all memory locations are on even address boundaries and byte instructions can address either the even or odd byte. The memory space is 65,536 bytes or 32,768 words. The word and byte formats are shown in Figure 3.

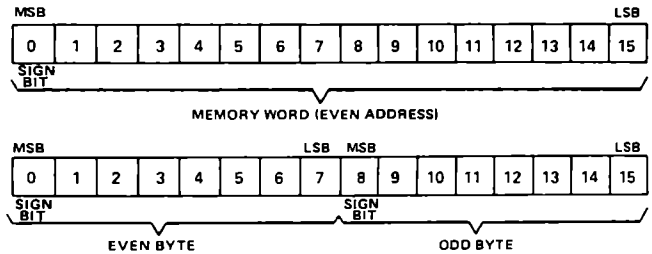


FIGURE 3 – WORD AND BYTE FORMATS

2.1 REGISTERS AND MEMORY

The 9900 employs an advanced memory-to-memory architecture. Blocks of memory designated as workspace replace internal-hardware registers with program-data registers. The 9900 memory map is shown in Figure 4. The first 32 words are used for interrupt trap vectors. The next contiguous block of 32 memory words is used by the extended operation (XOP) instruction for trap vectors. The last two memory words, $FFFC_{16}$ and $FFFE_{16}$, are used for the trap vector of the LOAD signal. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory.

Three internal registers are accessible to the user. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented. The status register (ST) contains the present state of the processor and will be further defined in Section 3.4. The workspace pointer (WP) contains the address of the first word in the currently active set of workspace registers.

A workspace-register file occupies 16 contiguous memory words in the general memory area (see Figure 4). Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or index registers. During instruction execution, the processor addresses any register in the workspace by adding the register number to the contents of the workspace pointer and initiating a memory request for the word. The relationship between the workspace pointer and its corresponding workspace is shown in Figure 5.

The workspace concept is particularly valuable during operations that require a context switch which is a change from one program environment to another (as in the case of an interrupt) or to a subroutine. Such an operation, using a conventional multi-register arrangement, requires that at least part of the contents of the register file be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the program counter, status register, and workspace pointer in the 9900 concept accomplishes a complete context switch withonly three store cycles and three fetch cycles. See Figure 5. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use in the new routine. A corresponding time saving occurs when the original context is restored. Instructions in the 9900 that result in a context switch include:

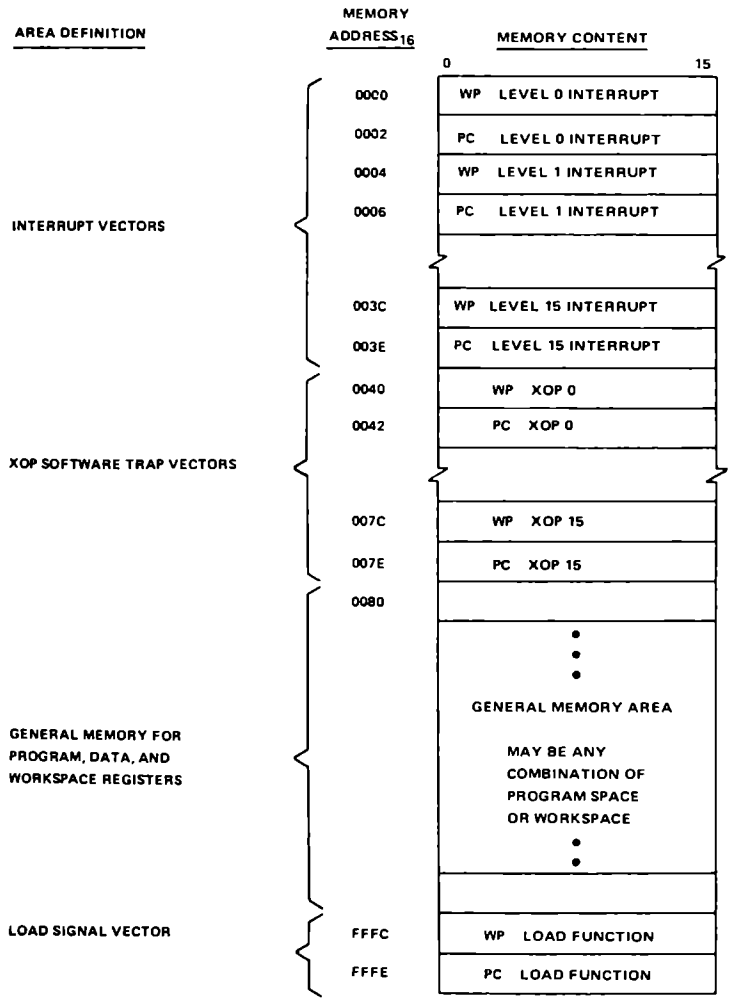


FIGURE 4 – MEMORY MAP

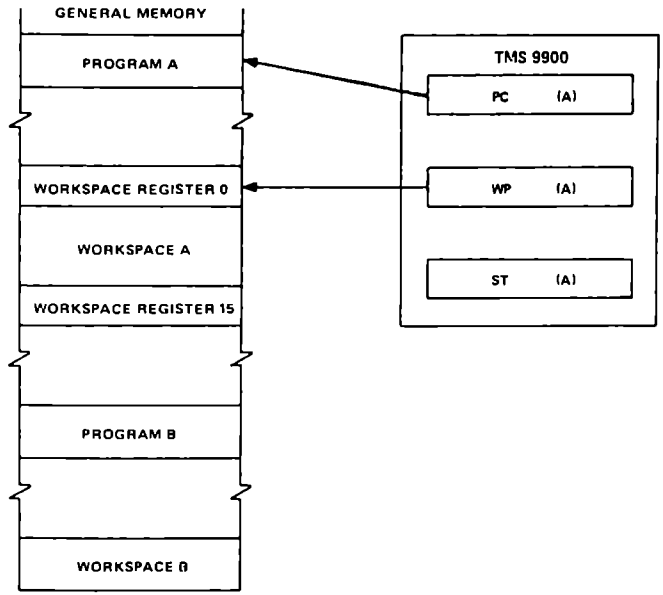


FIGURE 5 – MEMORY-TO-MEMORY WORKSPACE CONCEPT

1. Branch and Load Workspace Pointer (BLWP)
2. Return from Subroutine (RTWP)
3. Extended Operation (XOP).

Device interrupts, $\overline{\text{RESET}}$, and $\overline{\text{LOAD}}$ also cause a context switch by forcing the processor to trap to a service subroutine.

2.2 INTERRUPTS

The 9900 employs 16 interrupt levels with the highest priority level 0 and lowest level 15. Level 0 is reserved for the $\overline{\text{RESET}}$ function and all other levels may be used for external devices. The external levels may also be shared by several device interrupts, depending upon system requirements.

The 9900 continuously compares the interrupt code (IC0 through IC3) with the interrupt mask contained in status-register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the processor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. Then, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15, respectively, of the new workspace. The 9900 then forces the interrupt mask to a value that is one less than the level of the interrupt being serviced, except for level-zero interrupt, which loads zero into the mask. This allows

only interrupts of higher priority to interrupt a service routine. The processor also inhibits interrupts until the first instruction of the service routine has been executed to preserve program linkage should a higher priority interrupt occur. All interrupt requests should remain active until recognized by the processor in the device-service routine. The individual service routines must reset the interrupt requests before the routine is complete.

If a higher priority interrupt occurs, a second context switch occurs to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower-priority interrupt. All interrupt subroutines should terminate with the return instruction to restore original program parameters. The interrupt-vector locations, device assignment, enabling-mask value, and the interrupt code are shown in Table 1.

TABLE 1
INTERRUPT LEVEL DATA

Interrupt Level	Vector Location (Memory Address In Hex)	Device Assignment	Interrupt Mask Values To Enable Respective Interrupts (ST12 thru ST15)	Interrupt Codes IC0 thru IC3
(Highest priority) 0	00	Reset	0 through F*	0000
1	04	External device	1 through F	0001
2	08		2 through F	0010
3	0C		3 through F	0011
4	10		4 through F	0100
5	14		5 through F	0101
6	18		6 through F	0110
7	1C		7 through F	0111
8	20		8 through F	1000
9	24		9 through F	1001
10	28		A through F	1010
11	2C		B through F	1011
12	30		C through F	1100
13	34		D through F	1101
14	38		E and F	1110
(Lowest priority) 15	3C	External device	F only	1111

* Level 0 can not be disabled

The 9900 interrupt interface utilizes standard TTL components as shown in Figure 6. Note that for eight or less external interrupts a single SN54/74148 is required and for one external interrupt $\overline{\text{INTREQ}}$ is used as the interrupt signal with a hard-wired code IC0 through IC3.

2.3 I/O INTERFACE COMMUNICATIONS-REGISTER-UNIT (CRU)

The SBP 9900 communications-register-unit (CRU) is a versatile, direct command-driven serial I/O interface. The CRU may directly address, in bit-fields of one to sixteen, up to 4096 peripheral input bits and up to 4096 peripheral output bits. The SBP 9900 executes three single-bit and two multiple-bit CRU instructions. The single-bit instructions include TEST BIT (TB), SET BIT TO ONE (SBO), and SET BIT TO ZERO (SBZ); the multiple-bit instructions include LOAD CRU (LDCR) and STORE CRU (STCR).

The SBP 9900 employs three dedicated I/O signals CRUIN, CRUOUT, CRUCLK, and the least significant twelve bits of the address bus to support the CRU interface. CRU interface timing is shown in Section 2.9.

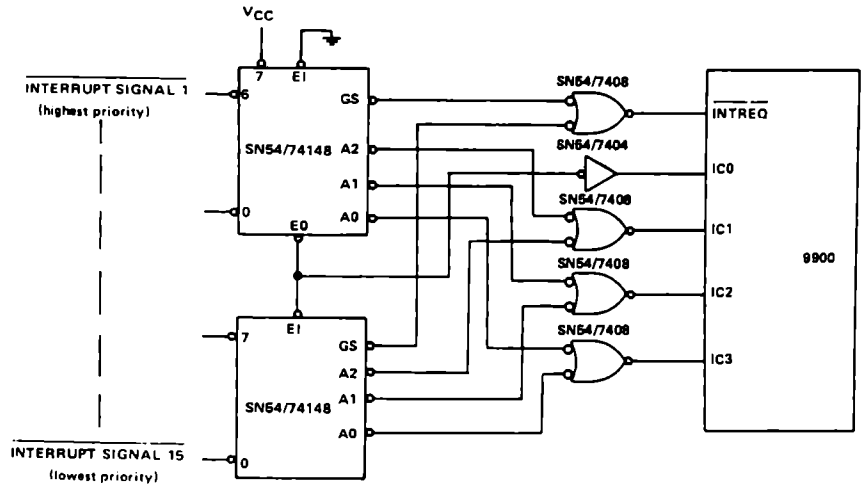


FIGURE 6 – 9900 INTERRUPT INTERFACE

2.4 SINGLE-BIT CRU OPERATIONS

The 9900 performs three single-bit CRU functions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the 9900 develops a CRU-bit address and places it on the address bus, A3 to A14.

For the two output operations (SBO and SBZ), the processor also generates a CRUCLK pulse, indicating an output operation to the CRU device, and places bit 7 of the instruction word on the CRUOUT line to accomplish the specified operation (bit 7 is a one for SBO and a zero for SBZ). A test-bit instruction transfers the addressed CRU bit from the CRUIN input line to bit 2 of the status register (EQUAL).

The 9900 develops a CRU-bit address for the single-bit operations from the CRU-base address contained in workspace register 12 and the signed displacement count contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from W12 is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 7 illustrates the development of a single-bit CRU address.

2.5 MULTIPLE-BIT CRU OPERATIONS

The 9900 performs two multiple-bit CRU operations: store communications register (STCR) and load communications register (LDCR). Both operations perform a data transfer from the CRU-to-memory or from memory-to-CRU as illustrated in Figure 8. Although the figure illustrates a full 16-bit transfer operation, any number of bits from 1 through 16 may be involved. The LDCR instruction fetches a word from memory and right-shifts it to serially transfer it to CRU output bits. If the LDCR involves eight or fewer bits, those bits come from the right-justified field within the addressed byte of the memory word. If the LDCR involves nine or more bits, those bits come from the right-justified field within the whole memory word. When transferred to the CRU interface, each successive bit receives an address that is sequentially greater than the address for the previous bit. This addressing mechanism results

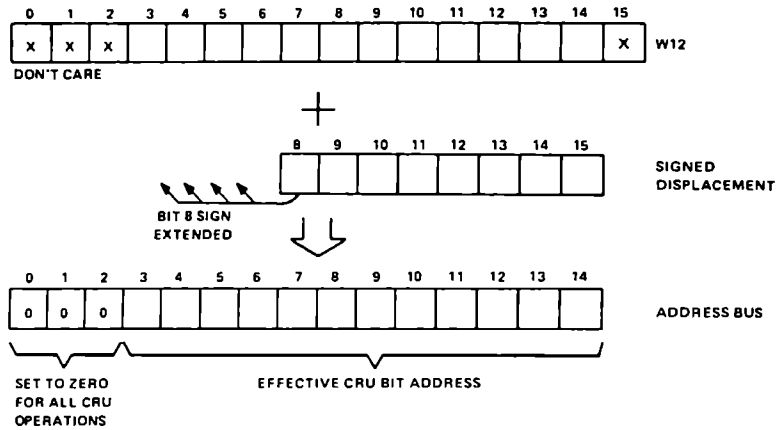

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
X X X X
W12
DON'T CARE
8 9 10 11 12 13 14 15
SIGNED DISPLACEMENT
BIT 8 SIGN EXTENDED
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14
0 0 0
ADDRESS BUS
SET TO ZERO FOR ALL CRU OPERATIONS
EFFECTIVE CRU BIT ADDRESS

FIGURE 7 – 9900 SINGLE-BIT CRU ADDRESS DEVELOPMENT

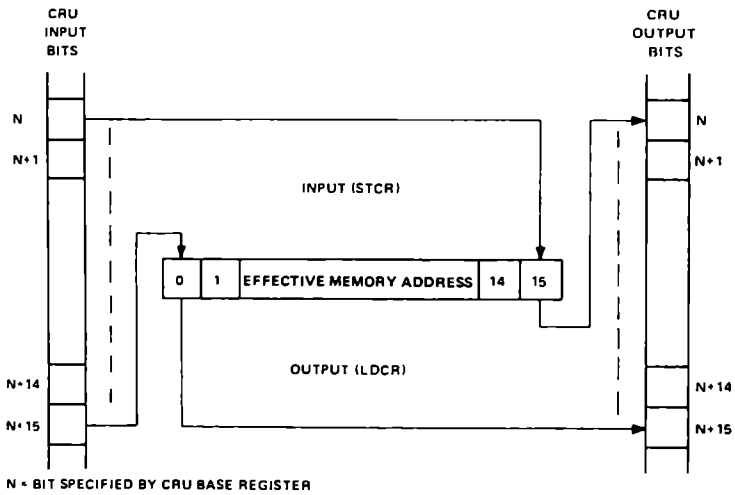


FIGURE 8 – 9900 LDCR/STCR DATA TRANSFERS

in an order reversal of the bits; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressed bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

An STCR instruction transfers data from the CRU to memory. If the operation involves a byte or less transfer, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves from nine to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to

zero. When the input from the CRU device is complete, the first bit from the CRU is the least-significant-bit position in the memory word or byte.

Figure 9 illustrates how to implement a 16-bit input and a 16-bit output register in the CRU interface. CRU addresses are decoded as needed to implement up to 256 such 16-bit interface registers. In system application, however, only the exact number of interface bits needed to interface specific peripheral devices are implemented. It is not necessary to have a 16-bit interface register to interface an 8-bit device.

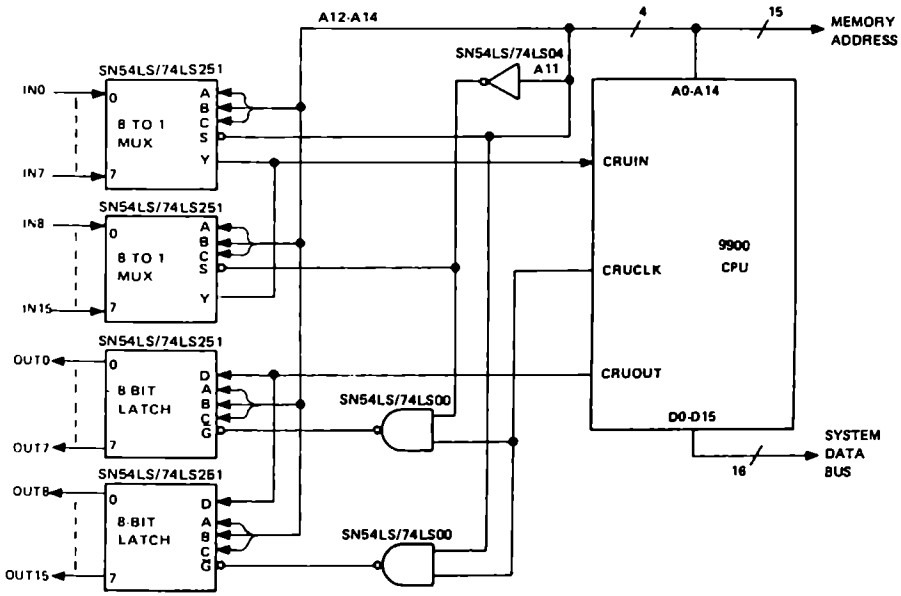


FIGURE 9 – 9900 16-BIT INPUT/OUTPUT INTERFACE

2.6 EXTERNAL INSTRUCTIONS

The 9900 has five external instructions that allow user-defined external functions to be initiated under program control. These instructions are CKON, CKOF, RSET, IDLE, and LREX. These mnemonics, except for IDLE, relate to functions implemented in the 990 minicomputer and do not restrict use of the instructions to initiate various user-defined functions. IDLE also causes the 9900 to enter the idle state and remain until an interrupt, $\overline{\text{RESET}}$, or $\overline{\text{LOAD}}$ occurs. When any of these five instructions are executed by the 9900, a unique 3-bit code appears on the most-significant 3 bits of the address bus (A0 through A2) along with a CRUCLK pulse. When the 9900 is in an idle state, the 3-bit code and CRUCLK pulses occur repeatedly until the idle state is terminated. The codes are shown in Table 2.

Figure 10 illustrates typical external decode logic to implement these instructions. Note that a signal is generated to inhibit CRU decodes during external instructions.

TABLE 2
EXTERNAL INSTRUCTIONS

EXTERNAL INSTRUCTION	A0	A1	A2
LREX	H	H	H
CKOF	H	H	L
CKON	H	L	H
RSET	L	H	H
IDLE	L	H	L

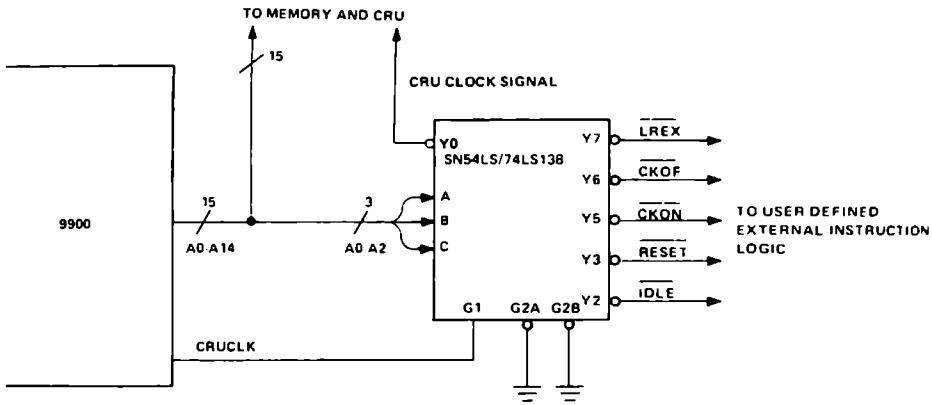


FIGURE 10 – EXTERNAL INSTRUCTION DECODE LOGIC

2.7 LOAD FUNCTION

The $\overline{\text{LOAD}}$ signal allows cold-start ROM loaders and front panels to be implemented for the 9900. When active, $\overline{\text{LOAD}}$ causes the 9900 to initiate an interrupt sequence immediately following the instruction being executed. Memory location FFC is used to obtain the vector (WP and PC). The old PC, WP and ST are loaded into the new workspace and the interrupt mask is set to 0000. Then, program execution resumes using the new PC and WP.

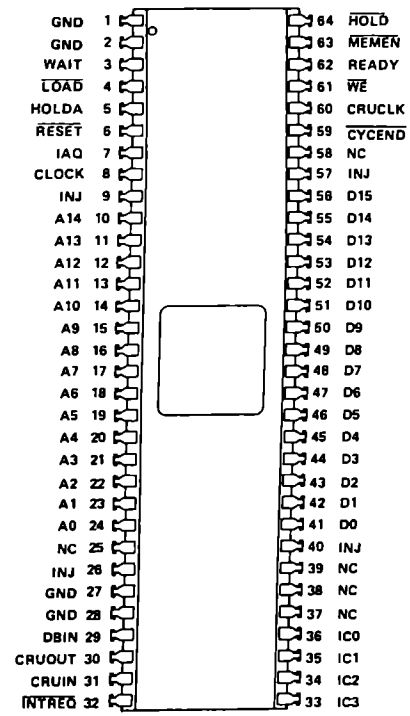
2.8 SBP 9900 PIN DESCRIPTION

Table 3 describes the function of each SBP 9900 pin, and Figure 11 illustrates their assigned locations.

TABLE 3
9900 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
			ADDRESS BUS
A0 (MSB)	24	OUT	A0 (MSB) through A14 (LSB) comprise the address bus. This open-collector bus provides the memory-address vector to the external-memory system when $\overline{\text{MEMEN}}$ is active, and I/O-bit addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive. When HOLDA is active, the address bus is pulled to the logic level HIGH state by the individual pull-up resistors tied to each respective
A14 (LSB)	10	OUT	open-collector output.
			DATA BUS
D0 (MSB)	41	I/O	D0 (MSB) through D15 (LSB) comprise the bidirectional open-collector data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when $\overline{\text{MEMEN}}$ is active. When HOLDA is active, the data bus is pulled to the logic level HIGH state by the individual pull-up resistors tied to each
D15 (LSB)	56	I/O	respective open-collector output.
			POWER SUPPLY
INJ	9		Injector-Supply-Current
INJ	26		Injector-Supply-Current
INJ	40		Injector-Supply-Current
INJ	57		Injector-Supply-Current
GND	1		Ground Reference
GND	2		Ground Reference
GND	27		Ground Reference
GND	28		Ground Reference
			CLOCK
CLOCK	8	IN	CLOCK
			BUS CONTROL
DBIN	29	OUT	DATA BUS IN. When active (pulled to logic level HIGH), DBIN indicates that the SBP 9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains at logic level LOW in all other cases except when HOLDA is active (pulled to logic level HIGH).
$\overline{\text{MEMEN}}$	63	OUT	MEMORY ENABLE. When active (logic level LOW), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address.
$\overline{\text{WE}}$	61	OUT	WRITE ENABLE. When active (logic level LOW), $\overline{\text{WE}}$ indicates that the SBP 9900 data bus is outputting data to be written into memory.

FIGURE 11 – SBP 9900 PIN ASSIGNMENTS.



NC–No Internal connection

TABLE 3 (CONTINUED)

SIGNATURE	PIN	I/O	DESCRIPTION
CRUCLK	60	OUT	COMMUNICATIONS-REGISTER-UNIT (CRU) CLOCK. When active (pulled to logic level HIGH), CRUCLK indicates to the external interface logic the presence of output data on CRUOUT, or the presence of an encoded external instruction on A0 through A2.
CRUIN	31	IN	CRU DATA IN. CRUIN, normally driven by 3-state or open-collector devices, receives input data from the external interface logic. When the SBP 9900 executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU DATA OUT. CRUOUT outputs serial data when the SBP 9900 executes a LDCR, SBZ, SBO instruction. The data on CRUOUT should be sampled by the external interface logic when CRUCLK goes active (pulled to logic level HIGH).
			INTERRUPT CONTROL
$\overline{\text{INTREQ}}$	32	IN	INTERRUPT REQUEST. When active (logic level LOW), $\overline{\text{INTREQ}}$ indicates that an external interrupt is requesting service. If $\overline{\text{INTREQ}}$ is active, the SBP 9900 loads the data on the interrupt-code input lines IC0 through IC3 into the internal interrupt-code storage register. The code is then compared to the interrupt mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15), the SBP 9900 initiates the interrupt sequence. If the comparison fails, the SBP 9900 ignores the interrupt request. In that case, $\overline{\text{INTREQ}}$ should be held active. The SBP 9900 will continue to sample IC0 through IC3 until the program enables a sufficiently low interrupt-level to accept the requesting interrupt.
IC0 (MSB)	36	IN	INTERRUPT CODES. IC0 (MSB) through IC3 (LSB), receiving an interrupt identity code, are sampled by the SBP 9900 when $\overline{\text{INTREQ}}$ is active (logic level LOW). When IC0 through IC3 are LLLH, the highest priority *external* interrupt is requesting service; when HHHH, the lowest priority external interrupt is requesting service.
IC0 (LSB)	33	IN	
			MEMORY CONTROL
$\overline{\text{HOLD}}$	64	IN	When active (logic level LOW), $\overline{\text{HOLD}}$ indicates to the SBP 9900 that an external controller (e.g., DMA device) desires to use both the address bus and data bus to transfer data to or from memory. In response, the SBP 9900 enters the hold state after completion of its present memory cycle. The SBP 9900 then allows its address bus, data bus, $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, DBIN, and HOLDA facilities to be pulled to the logic level HIGH state. When $\overline{\text{HOLD}}$ is deactivated, the SBP 9900 returns to normal operation from the point at which it was stopped.
HOLDA	5	OUT	HOLD ACKNOWLEDGE. When active (pulled to logic level HIGH), HOLDA indicates that the SBP 9900 is in the hold state and that its address bus, data bus, $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN facilities are pulled to the logic level HIGH state.
READY	62	IN	When active (logic level HIGH), READY indicates that the memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the SBP 9900 enters a wait state and suspends internal operation until the memory systems activate READY.
WAIT	3	OUT	When active (pulled to logic level HIGH), WAIT indicates that the SBP 9900 has entered a wait state in response to a not-ready condition from memory.
			TIMING AND CONTROL
IAQ	7	IN	INSTRUCTION ACQUISITION. IAQ is active (pulled to logic level HIGH) during any SBP 9900 initiated instruction acquisition memory cycle. Consequently, IAQ may be used to facilitate detection of illegal op codes.
$\overline{\text{CYCEND}}$	59	OUT	CYCLE END. When active (logic level LOW), $\overline{\text{CYCEND}}$ indicates that the SBP 9900 will initiate a new microinstruction cycle on the low-to-high transition of the next CLOCK.
$\overline{\text{LOAD}}$	4	IN	When active (logic level LOW), $\overline{\text{LOAD}}$ causes the SBP 9900 to execute a nonmaskable interrupt with memory addresses $FFFC_{16}$ and $FFFE_{16}$ containing the associated trap vectors (WP and PC). The load sequence is initiated after the instruction being executed is completed. $\overline{\text{LOAD}}$ will also terminate an idle state. If $\overline{\text{LOAD}}$ is active during the time $\overline{\text{RESET}}$ is active, the $\overline{\text{LOAD}}$ trap will occur after the RESET function is completed. $\overline{\text{LOAD}}$ should remain active for one instruction execution period (IAQ may be

TABLE 3 (CONCLUDED)

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{\text{LOAD}}$ (Cont.)			used to monitor instruction boundaries). $\overline{\text{LOAD}}$ may be used to implement cold-start ROM loaders. Additionally, front-panel routines may be implemented using CRU bits as front-panel-interface signals, and software-control routines to direct the panel operations.
$\overline{\text{RESET}}$	6	IN	When active (logic level LOW), $\overline{\text{RESET}}$ causes the SBP 9900 to reset itself and inhibit $\overline{\text{WE}}$ and CRUCLK. When $\overline{\text{RESET}}$ is released, the SBP 9900 initiates a level-zero interrupt sequence acquiring the WP and PC trap vectors from memory locations 0000_{16} and 0002_{16}, sets all status register bits to logic level LOW, and then fetches the first instruction of the reset program environment. $\overline{\text{RESET}}$ must be held active for a minimum of three CLOCK cycles.

2.9 SBP 9900 TIMING

2.9.1 SBP 9900 MEMORY

The SBP 9900 basic memory timing for a memory-read cycle with no wait states, and a memory-write cycle with one wait state, is as shown in Figure 12. During each memory-read or memory-write cycle, $\overline{\text{MEMEN}}$ becomes active (logic level LOW) along with valid memory-address data appearing on the address bus (A0 through A14).

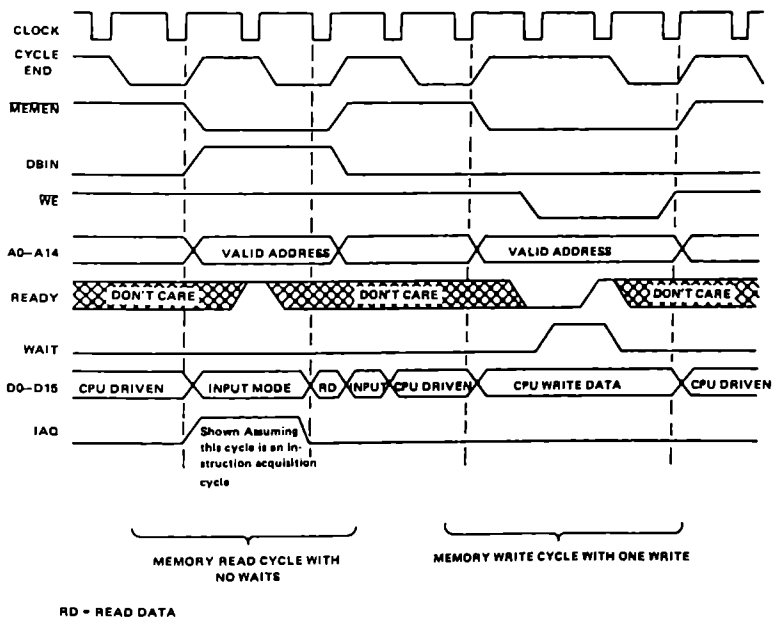


FIGURE 12 – SBP 9900 MEMORY BUS TIMING

In the case of a memory-read cycle, DBIN becomes active (pulled to logic level HIGH) at the same time memory-address data becomes valid; the memory write strobe $\overline{WE}$ remains inactive (pulled to logic level HIGH). If the memory-read cycle is initiated for acquisition of an instruction, IAQ becomes active (pulled to logic level HIGH) at the same time $\overline{MEMEN}$ becomes active. At the end of a memory-read cycle, $\overline{MEMEN}$ and DBIN together become inactive. At that time, though the address may change, the data bus remains in the input mode until terminated by the next high-to-low transition of the clock.

In the case of a memory-write cycle, $\overline{WE}$ becomes active (logic level LOW) with the first high-to-low transition of the clock after $\overline{MEMEN}$ becomes active; DBIN remains inactive. At the end of a memory-write cycle, $\overline{WE}$ and $\overline{MEMEN}$ together become inactive.

During either a memory-read or a memory-write operation, READY may be used to extend the duration of the associated memory cycle such that the speed of the memory system may be coordinated with the speed of the SBP 9900. If READY is inactive (logic level LOW) during the first low-to-high transition of the clock after $\overline{MEMEN}$ becomes active, the SBP 9900 will enter a wait state suspending further progress of the memory cycle. The first low-to-high transition of the clock after READY becomes active terminates the wait state and allows normal completion of the memory cycle.

2.9.2 SBP 9900 HOLD

The SBP 9900 hold facilities allow both the '9900 and external devices to share a common memory. To gain memory-bus control, an external device requiring direct memory access (DMA) sends a hold request ($\overline{HOLD}$) to the SBP 9900. When the next available non-memory cycle occurs, the SBP 9900 enters a hold state and signals its surrender of the memory-bus to the external device via a hold acknowledge (HOLDA). Receiving the hold acknowledgement, the external device proceeds to utilize the common memory. After its memory requirements have been satisfied, the external device returns memory-bus control to the SBP 9900 by releasing $\overline{HOLD}$.

When $\overline{HOLD}$ becomes active (logic level LOW), the SBP 9900 enters a hold state at the beginning of the next available non-memory cycle as shown below. Upon entering a hold state, HOLDA becomes active (pulled to logic level HIGH) with the following signals pulled to a HIGH logic level by the individual pull-up resistors tied to each respective open-collector output: DBIN, $\overline{MEMEN}$, $\overline{WE}$, A0 through A14, and D0 through D15. When $\overline{HOLD}$ becomes inactive, the SBP 9900 exits the hold state and regains memory-bus control. If $\overline{HOLD}$ becomes active during a CRU operation, the SBP 9900 uses an extra clock cycle after the deactivation of $\overline{HOLD}$ to reassert the CRU address thereby providing the normal setup time for the CRU-bit transfer.

2.9.3 SBP 9900 CRU

The transfer of two data-bits from memory to a peripheral CRU device, and the transfer of one data-bit from a peripheral CRU device to memory, is shown in Figure 14. To transfer a data-bit to a peripheral CRU device, the SBP 9900 outputs the corresponding CRU-bit-address on address bus bits A3 through A14 and the respective data-bit on CRUOUT. During the second clock cycle of the operation, the SBP 9900 outputs a pulse, on CRUCLK, indicating to the peripheral CRU device the presence of a data-bit. This process is repeated until transfer of the entire field of data-bits specified by the CRU instruction has been accomplished. To transfer a data-bit from a peripheral CRU device, the SBP 9900 outputs the corresponding CRU-bit-Address on address bus bits A3 through A14 and receives the respective data-bit on CRUIN. No CRUCLK pulses occur during a CRU input operation.

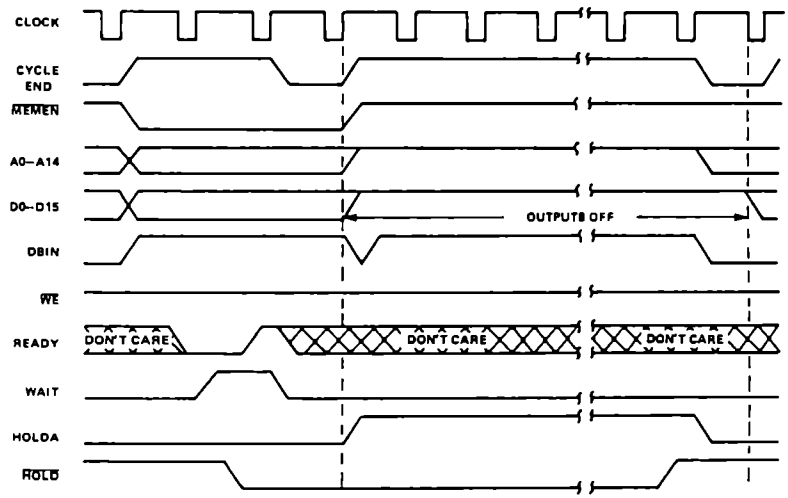


FIGURE 13 – SBP 9900 HOLD TIMING

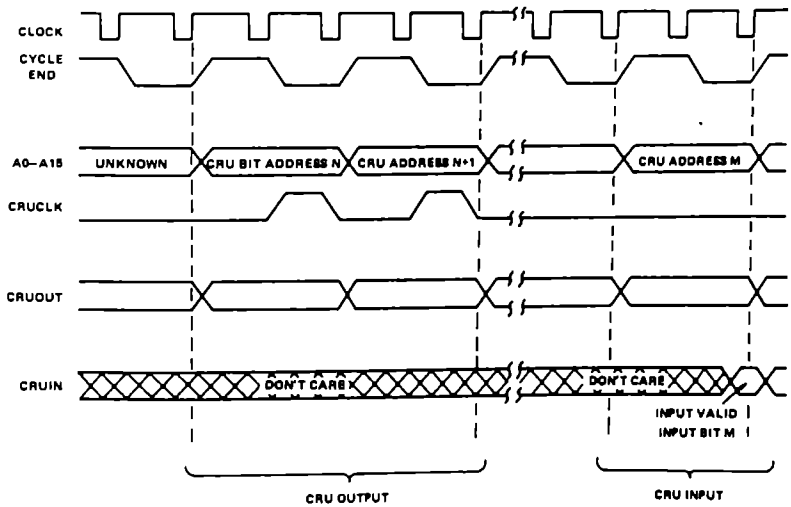


FIGURE 14 – SBP 9900 CRU INTERFACE TIMING

3. 9900 INSTRUCTION SET

3.1 DEFINITION

Each 9900 instruction performs one of the following operations:

- Arithmetic, logical, comparison, or manipulation operations on data
- Loading or storage of internal registers (program counter, workspace pointer, or status)
- Data transfer between memory and external devices via the CRU
- Control functions.

3.2 ADDRESSING MODES

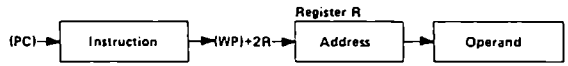
The 9900 instructions contain a variety of available modes for addressing random-memory data (e.g., program parameters and flags), or formatted memory data (character strings, data lists, etc.). The following figures graphically describe the derivation of the effective address for each addressing mode. The applicability of addressing modes to particular instructions is described in Section 3.5 along with the description of the operations performed by the instruction. The symbols following the names of the addressing modes [R, *R, *R+, @ LABEL, or @ TABLE (R)] are the general forms used by 9900 assemblers to select the addressing mode for register R.

3.2.1 WORKSPACE REGISTER ADDRESSING R

Workspace Register R contains the operand.

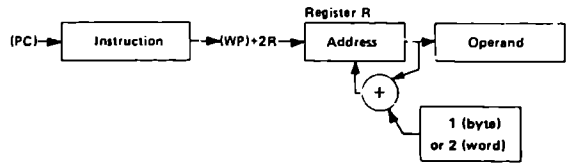
3.2.2 WORKSPACE REGISTER INDIRECT ADDRESSING *R

Workspace Register R contains the address of the operand.



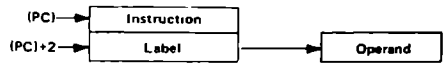
3.2.3 WORKSPACE REGISTER INDIRECT AUTO INCREMENT ADDRESSING *R+

Workspace Register R contains the address of the operand. After acquiring the operand, the contents of workspace register R are incremented.



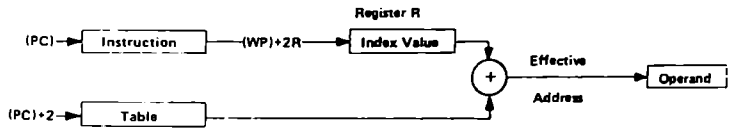
3.2.4 SYMBOLIC (DIRECT) ADDRESSING @ LABEL

The word following the instruction contains the address of the operand.



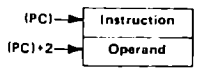
3.2.5 INDEXED ADDRESSING @ TABLE (R)

The word following the instruction contains the base address. Workspace register R contains the index value. The sum of the base address and the index value results in the effective address of the operand.



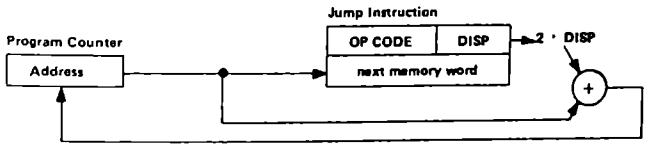
3.2.6 IMMEDIATE ADDRESSING

The word following the instruction contains the operand.



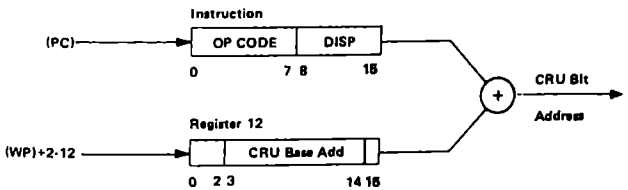
3.2.7 PROGRAM COUNTER RELATIVE ADDRESSING

The 8-bit signed displacement in the right byte (bits 8 through 15) of the instruction is multiplied by 2 and added to the updated contents of the program counter. The result is placed in the PC.



3.2.8 CRU RELATIVE ADDRESSING

The 8-bit signed displacement in the right byte of the instruction is added to the CRU base address (bits 3 through 14 of the workspace register 12). The result is the CRU address of the selected CRU bit.



3.3 TERMS AND DEFINITIONS

The terms used in describing the instructions of the 9900 are defined in Table 4.

TABLE 4
TERM DEFINITIONS

TERM	DEFINITION
B	Byte Indicator (1=byte, 0 = word)
C	Bit count
D	Destination address register
DA	Destination address
IOP	Immediate operand
LSB(n)	Least significant (right most) bit of (n)
MSB(n)	Most significant (left most) bit of (n)
N	Don't care
PC	Program counter
Result	Result of operation performed by instruction
S	Source address register
SA	Source address
ST	Status register
STn	Bit n of status register
T_D	Destination address modifier
T_S	Source address modifier
W	Workspace register
WRn	Workspace register n
(n)	Contents of n
a → b	a is transferred to b
|n|	Absolute value of n
+	Arithmetic addition
−	Arithmetic subtraction
AND	Logical AND
OR	Logical OR
⊕	Logical exclusive OR
$\bar{n}$	Logical complement of n

3.4 STATUS REGISTER

The status register contains the interrupt mask level and information pertaining to the instruction operation. Table 5 explains the bit indications.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ST0	ST1	ST2	ST3	ST4	ST5	ST6	not used (=0)					ST12	ST13	ST14	ST15
L>	A>	=	C	O	P	X						Interrupt Mask			

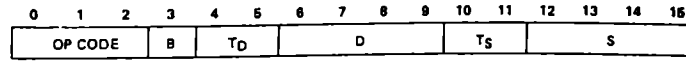
TABLE 5
STATUS REGISTER BIT DEFINITIONS

BIT	NAME	INSTRUCTION	CONDITION TO SET BIT TO 1
ST0	LOGICAL GREATER THAN	C,CB	If MSB(SA) = 1 and MSB(DA) = 0, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(W) = 1 and MSB of IOP = 0, or if MSB(W) = MSB of IOP and MSB of [IOP-(W)] = 1
		ABS	If (SA) ≠ 0
		All Others	If result ≠ 0
ST1	ARITHMETIC GREATER THAN	C,CB	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(W) = 0 and MSB of IOP = 1, or if MSB(W) = MSB of IOP and MSB of [IOP-(W)] = 1
		ABS	If MSB(SA) = 0 and (SA) ≠ 0
		All Others	If MSB of result = 0 and result ≠ 0
ST2	EQUAL	C, CB	If (SA) = (DA)
		CI	If (W) = IOP
		COC	If (SA) and $(\overline{DA})$ = 0
		CZC	If (SA) and (DA) = 0
		TB	If CRUIN = 1
		ABS	If (SA) = 0
		All Others	If result = 0
ST3	CARRY	A, AB, ABS, AI, DEC, DECT, INC, INCT, NEG, S, SB	If CARRY OUT = 1
		SLA, SRA, SRC, SRL	If last bit shifted out = 1
ST4	OVERFLOW	A, AB	If MSB(SA) = MSB(DA) and MSB of result ≠ MSB(DA)
		AI	If MSB(W) = MSB of IOP and MSB of result ≠ MSB(W)
		S, SB	If MSB(SA) ≠ MSB(DA) and MSB of result ≠ MSB(DA)
		DEC, DECT	If MSB(SA) = 1 and MSB of result = 0
		INC, INCT	If MSB(SA) = 0 and MSB of result = 1
		SLA	If MSB changes during shift
		DIV	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 0
		ABS, NEG	If (SA) = 8000_{16}
ST5	PARITY	CB, MOVB	If (SA) has odd number of 1's
		LDCR, STCR	If 1 ≤ C ≤ 8 and (SA) has odd number of 1's
		AB, SB, SOCB, SZCB	If result has odd number of 1's
ST6	XOP	XOP	If XOP instruction is executed
ST12–ST15	INTERRUPT MASK	LIMI	If corresponding bit of IOP is 1
		RTWP	If corresponding bit of WR15 is 1

3.5 INSTRUCTIONS

3.5.1 Dual Operand Instructions with Multiple Addressing Modes for Source and Destination Operand

General format:



If B = 1 the operands are bytes and the operand addresses are byte addresses. If B = 0 the operands are words and the operand addresses are word addresses.

The addressing mode for each operand is determined by the T field of that operand.

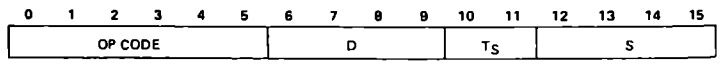
T_S OR T_D	S OR D	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	1
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	4
10	1, 2, . . . 15	Indexed	2,4
11	0, 1, . . . 15	Workspace register indirect auto-increment	3

NOTES. 1. When a workspace register is the operand of a byte instruction (bit 3 = 1), the left byte (bits 0 through 7) is the operand and the right byte (bits 8 through 15) is unchanged.
2. Workspace register 0 may not be used for indexing.
3. The workspace register is incremented by 1 for byte instructions (bit 3 = 1) and is incremented by 2 for word instructions (bit 3 = 0).
4. When $T_S = T_D = 10$, two words are required in addition to the instruction word. The first word is the source operand base address and the second word is the destination operand base address.

MNEMONIC	OP CODE 0 1 2	B 3	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
A	1 0 1	0	Add	Yes	0-4	(SA)+(DA) → (DA)
AB	1 0 1	1	Add bytes	Yes	0-5	(SA)+(DA) → (DA)
C	1 0 0	0	Compare	No	0-2	Compare (SA) to (DA) and set appropriate status bits
CB	1 0 0	1	Compare bytes	No	0-2,5	Compare (SA) to (DA) and set appropriate status bits
S	0 1 1	0	Subtract	Yes	0-4	(DA) − (SA) → (DA)
SB	0 1 1	1	Subtract bytes	Yes	0-5	(DA) − (SA) → (DA)
SOC	1 1 1	0	Set ones corresponding	Yes	0-2	(DA) OR (SA) → (DA)
SOCB	1 1 1	1	Set ones corresponding bytes	Yes	0-2,5	(DA) OR (SA) → (DA)
SZC	0 1 0	0	Set zeroes corresponding	Yes	0-2	(DA) AND $(\overline{SA})$ → (DA)
SZCB	0 1 0	1	Set zeroes corresponding bytes	Yes	0-2,5	(DA) AND $(\overline{SA})$ → (DA)
MOV	1 1 0	0	Move	Yes	0-2	(SA) → (DA)
MOVB	1 1 0	1	Move bytes	Yes	0-2,5	(SA) → (DA)

3.5.2 Dual Operand Instructions with Multiple Addressing Modes for the Source Operand and Workspace Register Addressing for the Destination

General format:



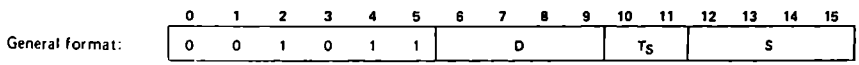
The addressing mode for the source operand is determined by the T_S field.

T_S	S	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	
10	1, 2, . . . 15	Indexed	1
11	0, 1, . . . 15	Workspace register indirect auto increment	2

NOTES. 1. Workspace register 0 may not be used for indexing.
2. The workspace register is incremented by 2.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
COC	0 0 1 0 0 0	Compare ones corresponding	No	2	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set ST2.
CZC	0 0 1 0 0 1	Compare zeros corresponding	No	2	Test (D) to determine if 0's are in each bit position where 1's are in (SA). If so, set ST2.
XOR	0 0 1 0 1 0	Exclusive OR	Yes	0-2	(D) ⊕ (SA) → (D)
MPY	0 0 1 1 1 0	Multiply	No		Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D+1 (least significant). If WR15 is D, the next word in memory after WR15 will be used for the least significant half of the product.
DIV	0 0 1 1 1 1	Divide	No	4	If unsigned (SA) is less than or equal to unsigned (D), perform no operation and set ST4. Otherwise, divide unsigned (D) and (D+1) by unsigned (SA). Quotient → (D), remainder → (D+1). If D = 15, the next word in memory after WR 15 will be used for the remainder.

3.5.3 Extended Operation (XOP) Instruction

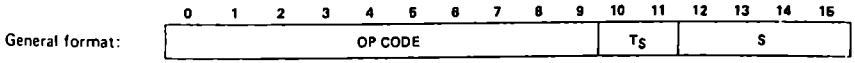


The T_S and S fields provide multiple mode addressing capability for the source operand. When the XOP is executed, ST6 is set and the following transfers occur:

$(40_{16} + 4D) \rightarrow$ (WP)
$(42_{16} + 4D) \rightarrow$ (PC)
SA → (new WR11)
(old WP) → (new WR13)
(old PC) → (new WR14)
(old ST) → (new WR15)

The 9900 does not test interrupt requests ($\overline{\text{INTREQ}}$) upon completion of the XOP instruction.

3.5.4 Single Operand Instructions



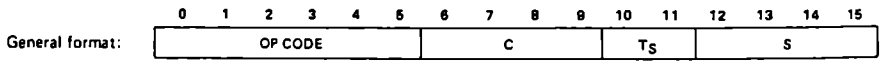
The T_S and S fields provide multiple mode addressing capability for the source operand.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
B	0 0 0 0 0 1 0 0 0 1	Branch	No	–	SA → (PC)
BL	0 0 0 0 0 1 1 0 1 0	Branch and link	No	–	(PC) → (WR11); SA → (PC)
BLWP	0 0 0 0 0 1 0 0 0 0	Branch and load workspace pointer	No	–	(SA) → (WP); (SA+2) → (PC); (old WP) → (new WR13); (old PC) → (new WR14); (old ST) → (new WR15); the interrupt input ($\overline{\text{INTREQ}}$) is not tested upon completion of the BLWP instruction.
CLR	0 0 0 0 0 1 0 0 1 1	Clear operand	No	–	0 → (SA)
SETO	0 0 0 0 0 1 1 1 0 0	Set to ones	No	–	$FFFF_{16}$ → (SA)
INV	0 0 0 0 0 1 0 1 0 1	Invert	Yes	0-2	$(\overline{SA})$ → (SA)
NEG	0 0 0 0 0 1 0 1 0 0	Negate	Yes	0-4	–(SA) → (SA)
ABS	0 0 0 0 0 1 1 1 0 1	Absolute value*	No	0-4	|(SA)| → (SA)
SWPB	0 0 0 0 0 1 1 0 1 1	Swap bytes	No	–	(SA), bits 0 thru 7 → (SA), bits 8 thru 15; (SA), bits 8 thru 15 → (SA), bits 0 thru 7.
INC	0 0 0 0 0 1 0 1 1 0	Increment	Yes	0-4	(SA) + 1 → (SA)
INCT	0 0 0 0 0 1 0 1 1 1	Increment by two	Yes	0-4	(SA) + 2 → (SA)
DEC	0 0 0 0 0 1 1 0 0 0	Decrement	Yes	0-4	(SA) – 1 → (SA)
DECT	0 0 0 0 0 1 1 0 0 1	Decrement by two	Yes	0-4	(SA) – 2 → (SA)
X†	0 0 0 0 0 1 0 0 1 0	Execute	No	–	Execute the instruction at SA.

* Operand is compared to zero for status bit.

† If additional memory words for the execute instruction are required to define the operands of the instruction located at SA, these words will be accessed from PC and the PC will be updated accordingly. The instruction acquisition signal (IAQ) will not be true when the 9900 accesses the instruction at SA. Status bits are affected in the normal manner for the instruction executed.

3.5.5 CRU Multiple-Bit Instructions

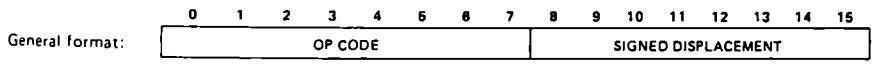


The C field specifies the number of bits to be transferred. If C = 0, 16 bits will be transferred. The CRU base register (WR12, bits 3 through 14) defines the starting CRU bit address. The bits are transferred serially and the CRU address is incremented with each bit transfer, although the contents of WR12 is not affected. T_S and S provide multiple mode addressing capability for the source operand. If 8 or fewer bits are transferred (C = 1 through 8), the source address is a byte address. If 9 or more bits are transferred (C = 0, 9 through 15), the source address is a word address. If the source is addressed in the workspace register indirect auto increment mode, the workspace register is incremented by 1 if C = 1 through 8, and is incremented by 2 otherwise.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
LDCR	0 0 1 1 0 0	Load communcation register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from (SA) to the CRU.
STCR	0 0 1 1 0 1	Store communcation register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from the CRU to (SA). Load unfilled bit positions with 0.

†ST5 is affected only if $1 \leq C \leq 8$.

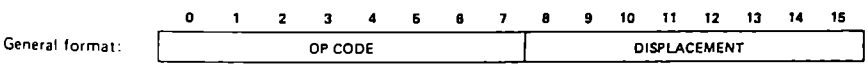
3.5.6 CRU Single-Bit Instructions



CRU relative addressing is used to address the selected CRU bit.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	STATUS BITS AFFECTED	DESCRIPTION
SBO	0 0 0 1 1 1 0 1	Set bit to one	–	Set the selected CRU output bit to 1.
SBZ	0 0 0 1 1 1 1 0	Set bit to zero	–	Set the selected CRU output bit to 0.
TB	0 0 0 1 1 1 1 1	Test bit	2	If the selected CRU input bit = 1, set ST2.

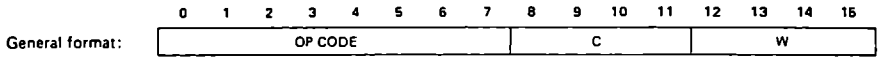
3.5.7 Jump Instructions



Jump instructions cause the PC to be loaded with the value selected by PC relative addressing if the bits of ST are at specified values. Otherwise, no operation occurs and the next instruction is executed since PC points to the next instruction. The displacement field is a word count to be added to PC. Thus, the jump instruction has a range of −128 to 127 words from memory-word address following the jump instruction. No ST bits are affected by jump instruction.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	ST CONDITION TO LOAD PC
JEQ	0 0 0 1 0 0 1 1	Jump equal	ST2 = 1
JGT	0 0 0 1 0 1 0 1	Jump greater than	ST1 = 1
JH	0 0 0 1 1 0 1 1	Jump high	ST0 = 1 and ST2 = 0
JHE	0 0 0 1 0 1 0 0	Jump high or equal	ST0 = 1 or ST2 = 1
JL	0 0 0 1 1 0 1 0	Jump low	ST0 = 0 and ST2 = 0
JLE	0 0 0 1 0 0 1 0	Jump low or equal	ST0 = 0 or ST2 = 1
JLT	0 0 0 1 0 0 0 1	Jump less than	ST1 = 0 and ST2 = 0
JMP	0 0 0 1 0 0 0 0	Jump unconditional	unconditional
JNC	0 0 0 1 0 1 1 1	Jump no carry	ST3 = 0
JNE	0 0 0 1 0 1 1 0	Jump not equal	ST2 = 0
JNO	0 0 0 1 1 0 0 1	Jump no overflow	ST4 = 0
JOC	0 0 0 1 1 0 0 0	Jump on carry	ST3 = 1
JOP	0 0 0 1 1 1 0 0	Jump odd parity	ST5 = 1

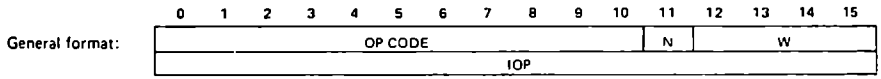
3.5.8 Shift Instructions



If C = 0, bits 12 through 15 of WR0 contain the shift count. If C = 0 and bits 12 through 15 of WR0 = 0, the shift count is 16.

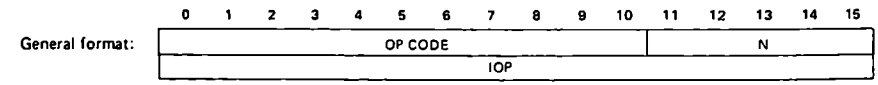
MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
SLA	0 0 0 0 1 0 1 0	Shift left arithmetic	Yes	0-4	Shift (W) left. Fill vacated bit positions with 0.
SRA	0 0 0 0 1 0 0 0	Shift right arithmetic	Yes	0-3	Shift (W) right. Fill vacated bit positions with original MSB of (W).
SRC	0 0 0 0 1 0 1 1	Shift right circular	Yes	0-3	Shift (W) right. Shift previous LSB into MSB.
SRL	0 0 0 0 1 0 0 1	Shift right logical	Yes	0-3	Shift (W) right. Fill vacated bit positions with 0's.

3.5.9 Immediate Register Instructions



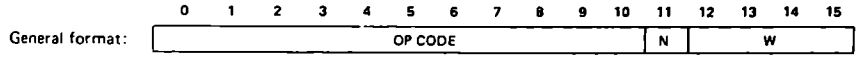
MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
AI	0 0 0 0 0 0 1 0 0 0 1	Add immediate	Yes	0-4	(W) + IOP → (W)
ANDI	0 0 0 0 0 0 1 0 0 1 0	AND immediate	Yes	0-2	(W) AND IOP → (W)
CI	0 0 0 0 0 0 1 0 1 0 0	Compare immediate	Yes	0-2	Compare (W) to IOP and set appropriate status bits
LI	0 0 0 0 0 0 1 0 0 0 0	Load immediate	Yes	0-2	IOP → (W)
ORI	0 0 0 0 0 0 1 0 0 1 1	OR immediate	Yes	0-2	(W) OR IOP → (W)

3.5.10 Internal Register Load Immediate Instructions



MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
LWPI	0 0 0 0 0 0 1 0 1 1 1	Load workspace pointer immediate	IOP → (WP), no ST bits affected
LIMI	0 0 0 0 0 0 1 1 0 0 0	Load interrupt mask	IOP, bits 12 thru 15 → ST12 thru ST15

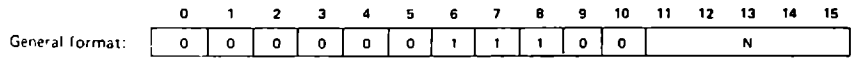
3.5.11 Internal Register Store Instructions



No ST bits are affected.

MNEMONIC	OP CODE	MEANING	DESCRIPTION
	0 1 2 3 4 5 6 7 8 9 10		
STST	0 0 0 0 0 0 1 0 1 1 0	Store status register	(ST) → (W)
STWP	0 0 0 0 0 0 1 0 1 0 1	Store workspace pointer	(WP) → (W)

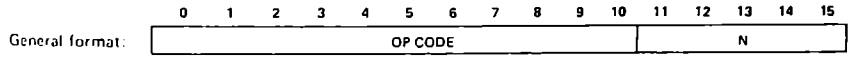
3.5.12 Return Workspace Pointer (RTWP) Instruction



The RTWP instruction causes the following transfers to occur:

(WR15) → (ST)
(WR14) → (PC)
(WR13) → (WP)

3.5.13 External Instructions



External instructions cause the three most-significant address lines (A0 through A2) to be set to the below-described levels and the CRUCLK line to be pulsed, allowing external control functions to be initiated.

MNEMONIC	OP CODE	MEANING	STATUS BITS AFFECTED	DESCRIPTION	ADDRESS BUS		
	0 1 2 3 4 5 6 7 8 9 10				A0	A1	A2
IDLE	0 0 0 0 0 0 1 1 0 1 0	Idle	–	Suspend TMS 9900 instruction execution until an interrupt, $\overline{\text{LOAD}}$, or $\overline{\text{RESET}}$ occurs	L	H	L
RSET	0 0 0 0 0 0 1 1 0 1 1	Reset	12–15	0 → ST12 thru ST15	L	H	H
CKOF	0 0 0 0 0 0 1 1 1 1 0	User defined		---	H	H	L
CKON	0 0 0 0 0 0 1 1 1 0 1	User defined		---	H	L	H
LREX	0 0 0 0 0 0 1 1 1 1 1	User defined		---	H	H	H

3.6 MICROINSTRUCTION CYCLE

The SBP 9900 includes circuitry which will indicate the completion of a microinstruction cycle. Designated as the $\overline{\text{CYCEND}}$ function, it provides CPU status that can simplify system design. The $\overline{\text{CYCEND}}$ output will go to a low logic level as a result of the low-to-high transition of each clock pulse which initiates the last clock of a microinstruction.

3.7 SBP 9900 INSTRUCTION EXECUTION TIMES

Instruction execution times for the SBP 9900 are a function of:

1) Clock cycle time, t_c

2) Addressing mode used where operands have multiple addressing mode capability

3) Number of wait states required per memory access.

The following Table 6 lists the number of clock cycles and memory accesses required to execute each SBP 9900 instruction. For instructions with multiple addressing modes for either or both operands, the table lists the number of clock cycles and memory accesses with all operands addressed in the workspace-register mode. To determine the additional number of clock cycles and memory accesses required for modified addressing, add the appropriate values from the referenced tables. The total instruction-execution time for an instruction is:

$$T = t_c (C + W \cdot M)$$

where:

T = total instruction execution time;
t_c = clock cycle time;
C = number of clock cycles for instruction execution plus address modification;
W = number of required wait states per memory access for instruction execution plus address modification;
M = number of memory accesses.

TABLE 6
INSTRUCTION EXECUTION TIMES

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	ADDRESS MODIFICATION† DEST
A	14	4	A	A
AB	14	4	B	B
ABS (MSB = 0)	12	2	A	
(MSB = 1)	14	3	A	
AI	14	4		
ANDI	14	4		
B	8	2	A	
BL	12	3	A	
BLWP	26	6	A	
C	14	3	A	A
CB	14	3	B	B
CI	14	3		
CKOF	12	1		
CKON	12	1		
CLR	10	3	A	
COC	14	3	A	
CZC	14	3	A	
DEC	10	3	A	
DECT	10	3	A	
DIV (ST4 is set)	16	3	A	
DIV (ST4 is reset)*	92-124	6	A	
IDLE	12	1		
INC	10	3	A	
INCT	10	3	A	
INV	10	3	A	
Jump (PC is changed)	10	1		
PC is not changed	8	1		
LDCR (C = 0)	52	3	A	
(1 ≤ C ≤ 8)	20+2C	3	B	
(9 ≤ C ≤ 15)	20+2C	3	A	
LI	12	3		
LIMI	14	2		
LREX	12	1		
RESET function	26	5		
LOAD function	22	5		
Interrupt context switch	22	5		

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	ADDRESS MODIFICATION† DEST
LWPI	10	2		
MOV	14	4	A	A
MOVB	14	4	B	B
MPY	52	5	A	
NEG	12	3	A	
ORI	14	4		
RSET	12	1		
RTWP	14	4		
S	14	4	A	A
SB	14	4	B	B
SBO	12	2		
SBZ	12	2		
SETO	10	3	A	
Shift (C = 0)	12+2C	3		
(C = 0, Bits 12-15 of WR0 = 0)	52	4		
(C = 0, Bits 12-15 of WR0 ≠ 0)	20+2n	4		
SOC	14	4	A	A
SOCB	14	4	B	B
STCR (C = 0)	60	4	A	
(1 ≤ C ≤ 7)	42	4	B	
(C = 8)	44	4	B	
(9 ≤ C ≤ 15)	58	4	A	
STST	8	2		
STWP	8	2		
SWPB	10	3	A	
SZC	14	4	A	A
SZCB	14	4	B	B
TB	12	2		
X**	4	1	A	
XOP	38	8	A	
XOR	14	4	A	
Undefined op codes 0000-01FF, 0320-03FF, 0C00-0FFF, 0780-07FF	6	1		

*Execution time is dependent upon the partial quotient after each clock cycle during execution.
**Execution time is added to the execution time of the instruction located at the source address minus 4 clock cycles and 1 memory access time.
†The letters A and B refer to the respective tables that follow.

ADDRESS MODIFICATION – TABLE A

ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	8	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D ≠ 0)	8	2

ADDRESS MODIFICATION – TABLE B

ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	6	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D ≠ 0)	8	2

As an example, the instruction MOVB is used in a system with $t_c = 0.333\ \mu s$ and no wait states are required to access memory. Both operands are addressed in the workspace register mode:

$$T = t_c\,(C + W \cdot M) = 0.333\,(14 + 0{\cdot}4)\ \mu s = 4.662\ \mu s$$

If two wait states per memory access were required, the execution time is:

$$T = 0.333\,(14 + 2{\cdot}4)\ \mu s = 7.326\ \mu s.$$

If the source operand was addressed in the symbolic mode and two wait states were required:

$$T = t_c\,(C + W \cdot M)$$
$$C = 14 + 8 = 22$$
$$M = 4 + 1 = 5$$
$$T = 0.333\,(22 + 2{\cdot}5)\ \mu s = 10.656\ \mu s.$$

4. INTERFACING

The input/output (I/O) accommodations have been designed for TTL compatibility. Direct interfacing, supportable by the entire families of catalog devices, is shown in Figure 15.

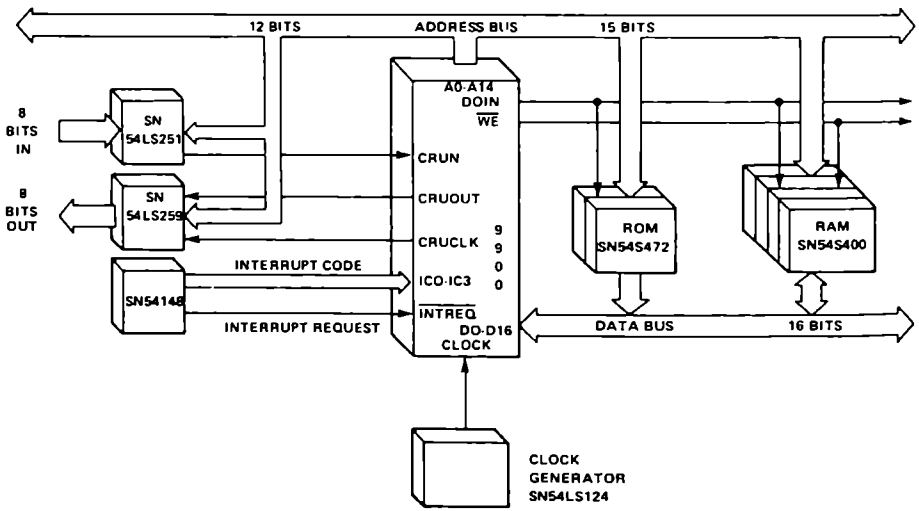


FIGURE 15 – MINIMUM SBP 9900 SYSTEM

4.1 INPUT CIRCUIT

The input circuit used on the SBP 9900 is basically an RTL configuration which has been modified for TTL compatibility as shown in Figure 16A. An input-clamping diode is incorporated to limit negative excursions (ringing) when the SBP 9900 is on the receiving end of a transmission line; an input switching threshold of nominally +1.5 volts has been specified for improved noise immunity. This threshold is achieved via two resistors which function as a voltage divider to increase the one V_{BE} threshold of the I^2L input transistor to +1.5 volts. Since this input circuit is independent of injector current, input threshold compatibility is maintained over the entire speed/power performance range.

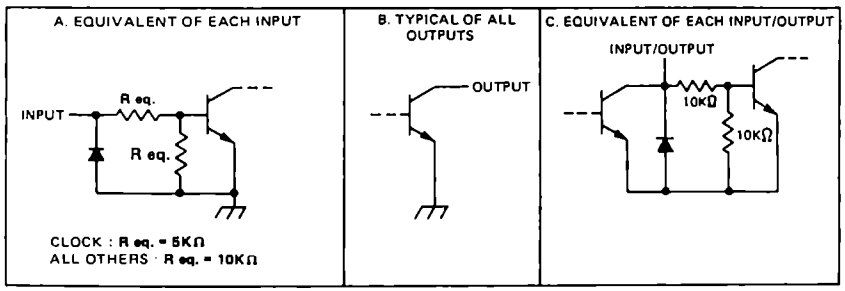


FIGURE 16 – SCHEMATICS OF EQUIVALENT INPUTS, OUTPUTS, INPUTS/OUTPUTS

The input circuit characteristics for input current versus input voltage are shown in Figure 17. The 10K and 20K ohm load lines and threshold knee at +1.5 volts provide a high-impedance characteristic to reduce input loading and improve the low-logic level input noise immunity over some standard TTL inputs. Full compatibility is maintained with virtually all 5 volt logic families even when the SBP 9900 is powered down (injector current reduced).

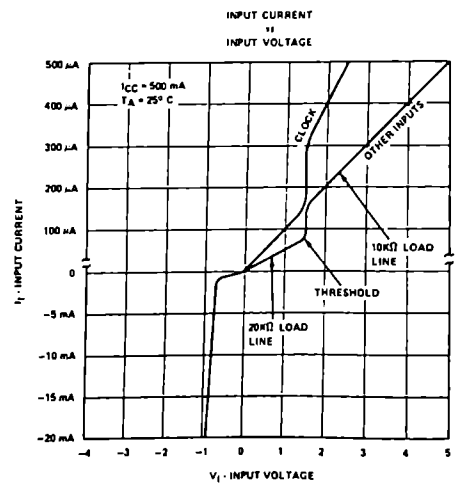


FIGURE 17 – TYPICAL INPUT CHARACTERISTICS

4.1.1 Sourcing Inputs

The inputs may be sourced directly by most 5 volt logic families. Five volt functions which feature internal pull-up resistors at their outputs require no external interface components; five volt functions which feature open-collector outputs generally require external pull-up resistors.

4.1.2 Terminating Unused Inputs

Inputs which are selected to be hardwired to a logic-level low may be connected directly to

ground. Inputs which are selected to be hardwired to a logic-level high must be tied, via a current limiting (pull-up) resistor, to a logic-level-high low-impedance voltage source such as V_{CC}. A single transient protecting resistor may be utilized common to (N) inputs.

4.2 OUTPUT CIRCUIT

The output circuit selected for the SBP 9900 is an injected open-collector transistor shown in Figure 16B. Since this transistor is injected, output sourcing capability is directly related to injector current. In other words, the number of loads which may be sourced by an SBP 9900 output is directly reduced as injector current is reduced.

The output circuit characteristic for logic-level low output voltage (V_{OL}) versus logic-level low output current (I_{OL}) is shown in Figure 18. At rated injector current, the SBP 9900 output circuit offers a low-level output voltage of typically 220 mV.

The output circuit characteristics for 1) logic-level high output voltage (V_{OH}) and current (I_{OH}), 2) rise times, and 3) next stage input noise immunity, are a function of the load circuit being sourced. The load circuit may be either:

A) the direct input, if no source current is required, of a five-volt logic family function,

or, for greater noise immunity and improved rise times,

B) the direct input of a five-volt logic family function in conjunction with a discrete pull-up resistor.

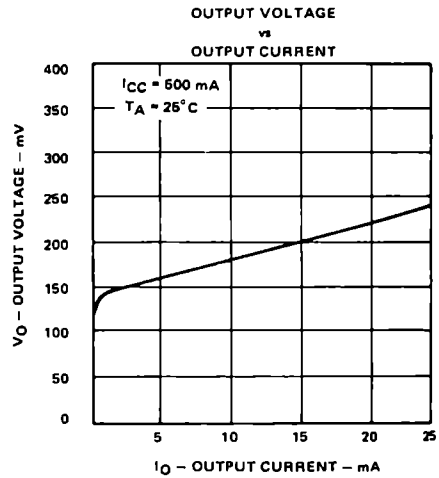


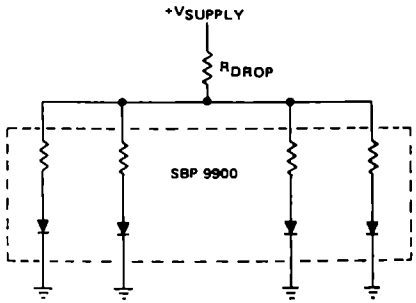
FIGURE 18 – TYPICAL OUTPUT CHARACTERISTICS

When a discrete pull-up resistor (R_L) is utilized, the fanout requirements placed on a particular SBP 9900 output restrict both the maximum and minimum value of R_L. Techniques for calculating $R_{L(max)}$ and $R_{L(min)}$ respectively are explained in the SBP 0400A, SBP 0401A data manual in Chapter 2 of this data book.

5. POWER SOURCE

I^2L is a current-injected logic. When placed across a curve tracer, the processor will resemble a silicon switching diode. Any voltage or current source capable of supplying the desired current at the injector node voltage required will suffice. A dry-cell battery, a 5-volt TTL power supply, a programmable current supply (for power-up/power-down operation) – literally whatever power source is convenient can be used for most cases. For example, if a 5-volt TTL power supply is to be used, a series dropping resistor would be connected between the 5-volt supply and the injector pins of the I^2L device, as illustrated in Figure 19, to select the desired operating current.

An alternate solution utilizes the Texas Instruments TL497 switching-regulator as illustrated in Figure 20.



GENERAL FORMULA (OHM'S LAW)

$$R_{DROP} = \frac{V_{SUPPLY} - V_{CC}}{I_{CC}}$$

EXAMPLE FOR V_{SUPPLY} = 5V, AND I_{CC} = 500 mA:

$$R_{DROP} = \frac{5 - 1.05}{0.5} = \frac{3.95}{0.5} = 7.9 \text{ OHMS}$$

FIGURE 19 – INJECTOR CURRENT CALCULATIONS

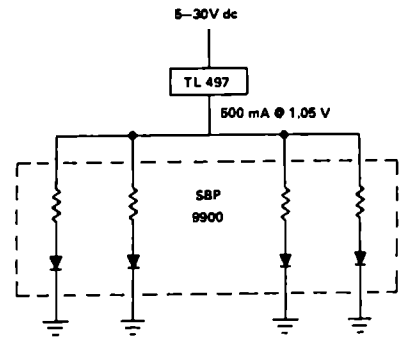


FIGURE 20 – SWITCHING-REGULATOR INJECTOR SOURCE

Operating from a constant current power source, the SBP 9900 may be powered-up/powered-down with complete maintenance of data integrity to execute instructions over a speed/power range spanning several orders of user-selectable injector-supply-current range as illustrated in Figure 21.

Figures 22 and 23 show the typical injector node voltages which occur across the temperature and injector current ranges.

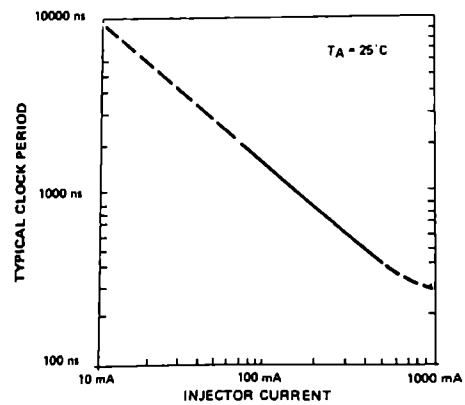


FIGURE 21 – SBP 9900 CLOCK PERIOD VS. INJECTOR CURRENT

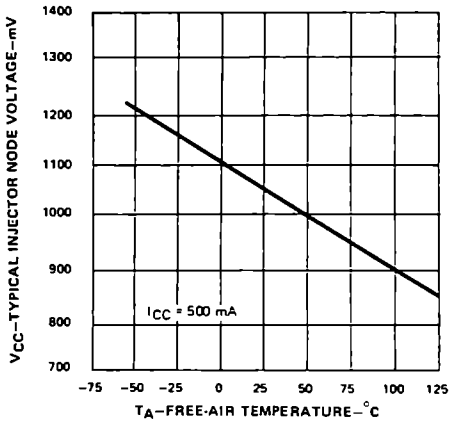


FIGURE 22 – INJECTOR-NODE VOLTAGE VS. FREE-AIR TEMPERATURE

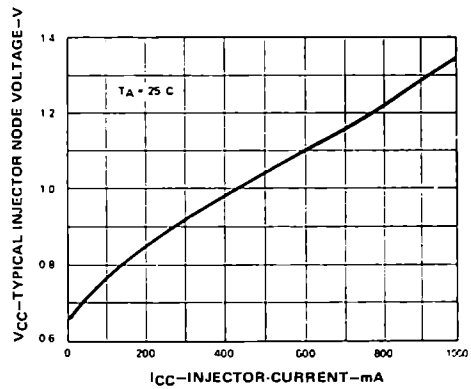


FIGURE 23 – INJECTOR-NODE VOLTAGE VS. INJECTOR CURRENT

6. ELECTRICAL AND MECHANICAL SPECIFICATIONS

6.1 SBP 9900 RECOMMENDED OPERATING CONDITIONS, UNLESS OTHERWISE NOTED I_{CC} = 500 mA

		MIN	NOM	MAX	UNIT
Supply current, I_{CC}		450	500	550	mA
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}				20	mA
Clock frequency, f_{clock}		0		2	MHz
Width of clock pulse, t_w	High (67%) (V_{IH} = 2.5 V max)	330			ns
	Low (33%)	170			
Clock rise time, t_r			10		ns
Clock fall time, t_f			10		ns
Setup time, t_{su} (see Figure 24)	$\overline{HOLD}$		160†		ns
	READY		90†		
	D0 – D15		45†		
	CRUIN		25†		
	$\overline{INTREQ}$		0†		
	IC0 – IC3		0†		
Hold time, t_h (see Figure 24)	$\overline{HOLD}$		0†		ns
	READY		30†		
	D0 – D15		30†		
	CRUIN		35†		
	$\overline{INTREQ}$		60†		
	IC0 – IC3		60†		
Operating free-air temperature, T_A		–55		125	°C

† Rising edge of clock pulse is reference.

6.2 SBP 9900 ELECTRICAL CHARACTERISTICS (OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE, UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		I_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current		I_{CC} = 500 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V V_{OH} = 5.5 V			400	μA
V_{OL}	Low-level output voltage		I_{CC} = 500 mA, V_{IL} = 0.8 V,	V_{IH} = 2 V I_{OL} = 20 mA			0.4	V
I_I	Input current	Clock	I_{CC} = 500 mA,	V_I = 2.4 V		480		μA
		All other inputs				240		

†For conditions shown as MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at I_{CC} = 500 mA, T_A = 25°C.

6.3 SBP 9900 SWITCHING CHARACTERISTICS (I_{CC} = 500 mA) SEE FIGURES 24 AND 25.

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
f_{max}	MAXIMUM CLOCK FREQUENCY		C_L = 150 pF, R_L = 280 Ω	2	2.6		MHz
t_{PLH} or t_{PHL}	CLOCK	ADDRESS BUS (A0 – A14)			170		ns
t_{PLH} or t_{PHL}	CLOCK	DATA BUS (D0 – D15)			170		ns
t_{PLH} or t_{PHL}	CLOCK	WRITE ENABLE ($\overline{WE}$)			220		ns
t_{PLH} or t_{PHL}	CLOCK	CYCLE END ($\overline{CYCEND}$)			170		ns
t_{PLH} or t_{PHL}	CLOCK	DATA BUS IN (DBIN)			190		ns
t_{PLH} or t_{PHL}	CLOCK	MEMORY ENABLE ($\overline{MEMEN}$)			155		ns
t_{PLH} or t_{PHL}	CLOCK	CRU CLOCK (CRUCK)			187		ns
t_{PLH} or t_{PHL}	CLOCK	CRU DATA OUT (CRUOUT)			210		ns
t_{PLH} or t_{PHL}	CLOCK	HOLD ACKNOWLEDGE (HLDA)			320		ns
t_{PLH} or t_{PHL}	CLOCK	WAIT			155		ns
t_{PLH} or t_{PHL}	CLOCK	INSTRUCTION ACQUISITION (IAQ)			155		ns

‡All typical values are at 25°C

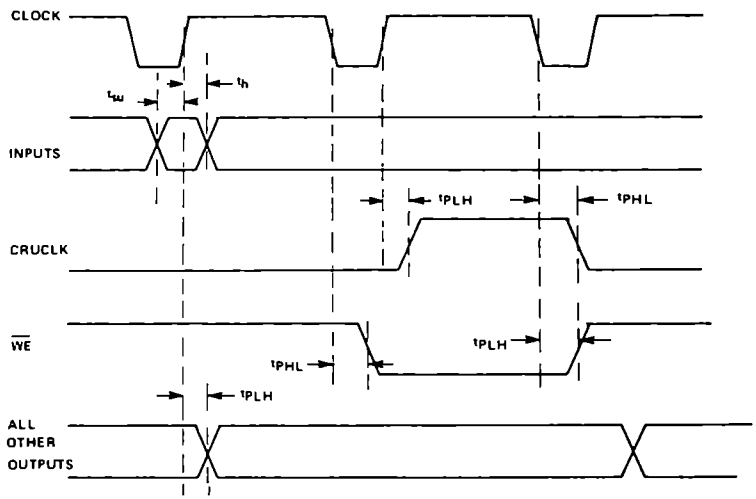


FIGURE 24 – SWITCHING TIMES-VOLTAGE WAVEFORMS

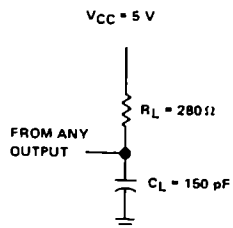


FIGURE 25 – SWITCHING TIMES LOAD CIRCUITS

6.4 CLOCK FREQUENCY VS. TEMPERATURE

Stability of the operational frequency over the full temperature range of −55°C to 125°C is illustrated in Figure 26.

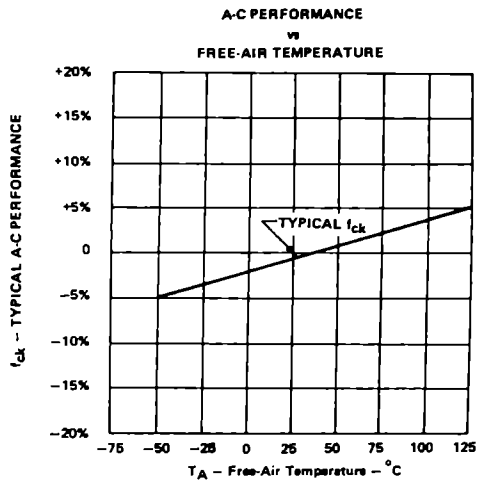
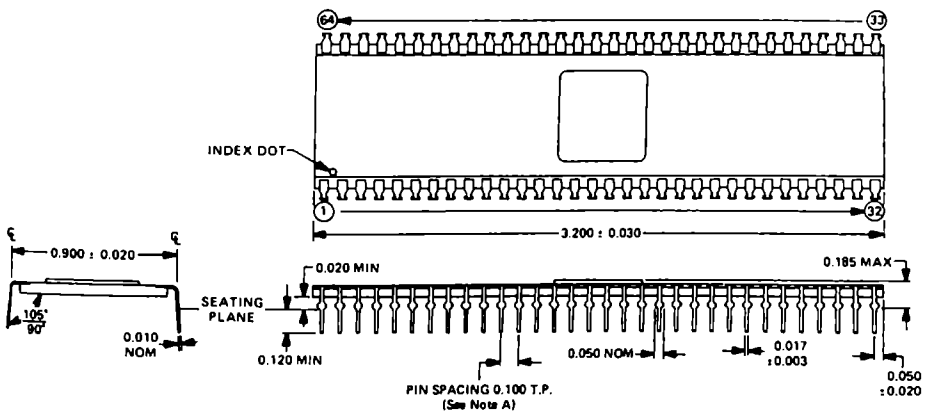


FIGURE 26 – A-C PERFORMANCE VS. TEMPERATURE

7. MECHANICAL DATA



NOTE A: Each pin centerline is located within 0.010 of its true longitudinal position.

8. SBP 9900 PROTOTYPING SYSTEM

8.1 HARDWARE

The TMS 9900 prototyping system enables the user to generate and debug software and to debug I/O controller interfaces. The prototyping system consists of:

- 990/4 computer with TMS 9900 microprocessor
- 1024 bytes of ROM containing the bootstrap loader for loading prototyping system software, the front-panel and maintenance utility, and the CPU self-testing feature
- 16,896 bytes of RAM with provisions for expansion up to 57,334 bytes of RAM
- Programmable-write-protect feature for RAM
- Interface for Texas Instruments Model 733 ASR* Electronic Data Terminal with provisions for up to five additional interface moculdes

* Requires remote device control and 1200 baud E.A interface option on 733 ASR.

- Available with Texas Instruments Model 733 ASR Electronic Data Terminal
- 7-inch-high table-top chassis
- Programmer's front panel with controls for run, halt, single-instruction execute, and entering and displaying memory or register contents
- Power supply with the following voltages:
  5 V dc @ 20 A
  12 V dc @ 2 A
  −12 V dc @ 1 A
  −5 V dc @ 0.1 A
- Complete hardware and software documentation.

8.2 SYSTEM CONSOLE

The system console for the prototyping system is the 733 ASR, which provides keyboard entry, 30-character-per-second thermal printer, and dual cassette drives for program loading and storage.

8.3 SOFTWARE

The following software is provided on cassette for loading into the prototyping system:

- Debug Monitor – Provides full control of the prototyping system during program development and includes single instruction, multiple breakpoints, and entry and display capability for register and memory contents for debugging user software under 733 ASR console control.
- One-Pass Assembler – Converts source code stored on cassette to relocatable object on cassette and generates program listing. (Object is upward compatible with other 990 series assemblers).
- Linking Loader – Allows loading of absolute and relocatable object modules and links object modules as they are loaded.
- Source Editor – Enables user modification of both source and object from cassette with resultant storage on cassette.
- Trace Routine – Allows user to monitor status of computer at completion of each instruction.
- PROM Programming/Documentation Facility – Provides documentation for ROM mask generation, or communicates directly with the optional PROM Programmer Unit.

The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

Bipolar Memory Data Manual

DECEMBER 1976

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INCORPORATED

INDEX FOR SCHOTTKY TTL BIPOLAR MEMORIES

FIELD PROGRAMMABLE READ-ONLY MEMORY (PROM) LINE SUMMARY (SEE PAGE 1)

MASK-PROGRAMMED READ-ONLY MEMORY (ROM) LINE SUMMARY

TYPE NUMBER (PACKAGES)		TYPE OF OUTPUT(S)	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		SEE PAGE
−55°C to 125°C	0° to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION	
SN5488A(J, W)	SN7488A(J, N)	Open-Collector	256 Bits (32 W x 8 B)	26 ns	320 mW	7
SN54187(J, W)	SN74187(J, N)	Open-Collector	1024 Bits (256 W x 4 B)	40 ns	460 mW	7
SN54S270(J)	SN74S270(J, N)	Open-Collector	2048 Bits (512 W x 4 B)	45 ns	525 mW	7
SN54S370(J)	SN74S370(J, N)	3-State				
SN54S271(J)	SN74S271(J, N)	Open-Collector	2048 Bits (256 W x 8 B)	45 ns	525 mW	7
SN54S371(J)	SN74S371(J, N)	3-State				

READ/WRITE MEMORY (RAM) LINE SUMMARY

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE		SEE PAGE
−55°C to 125°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION	
SN54S189(J, W)	SN74S189(J, N)	64 bits (16 W x 4B)	Three-state	25 ns	375 mW	15
SN54S289(J, W)	SN74S289(J, N)		Open-Collector			
SN54S200A(J, W)	SN74S200A(J, N)	256 bits (256 W x 1B)	Three-State	25 ns	600 mW	19
SN54LS200A(J, W)	SN74LS200A(J, N)			35 ns	275 mW	
SN54LS202(J, W)	SN74LS202(J, N)				275/100* mW	
SN54S300A(J, W)	SN74S300A(J, N)		Open-Collector	25 ns	600 mW	
SN54LS300A(J, W)	SN74LS300A(J, N)			35 ns	275 mW	
SN54LS302(J, W)	SN74LS302(J, N)				275/100* mW	
	SN74S214A(J, N)	1024 bits (1024 W x 1B)	Three-State	30 ns	550 mW	25
SN54S214(J)	SN74S214(J, N)			40 ns	550 mW	
SN54LS214(J)	SN74LS214(J, N)			65 ns	200 mW	
SN54LS215(J)	SN74LS215(J,N)			75 ns	200/100*mW	
	SN74S314A(J, N)		Open-Collector	30 ns	550 mW	
SN54S314(J)	SN74S314(J, N)			40 ns	550 mW	
SN54LS314(J)	SN74LS314(J, N)			75 ns	200 mW	
SN54LS315(J)	SN74S314(J, N)			75 ns	200/100*mW	
SN54S207(J)	SN74S207(J, N)	1024 bits (256 W x 4B)	Three-State	40 ns	600 mW	31
SN54LS207(J)	SN74LS207(J, N)			75 ns	200 mW	
SN54S208(J)	SN74S208(J,N)			40 ns	600 mW	
SN54LS208(J)	SN74LS208(J,N)			75 ns	200 mW	
SN54S400(J)	SN74S400(J, N)	4096 bits (4096 W x 1B)	Three-State	75 ns	500 mW	37
SN54S401(J)	SN74S401(J, N)		Open-Collector			

FIRST-IN/FIRST-OUT (FIFO) MEMORY

TYPE NUMBER (PACKAGES)	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE				SEE PAGE
		DATA RATES		FALL THROUGH	POWER DISSIPATION	
		INPUT	OUTPUT			
SN74S225(J, N)	80 bits (16 W x 5B)	d-c to 10 MHz	d-c to 10 MHz	215 ns	400 mW	39

*Powered down

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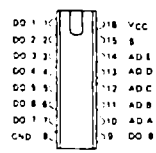
SCHOTTKY† PROM'S

SERIES 54S/74S PROGRAMMABLE READ-ONLY MEMORIES

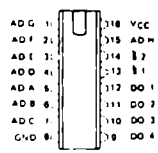
- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  - Fast Chip Select to Simplify System Decode
  - Choice of Three-State or Open-Collector Outputs
  - P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE	
−55°C to 125°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION
SN54S188(J, W)	SN74S188(J, N)	256 bits (32 W x 8 B)	open-collector	25 ns	400 mW
SN54S288(J, W)	SN74S288(J, N)		three-state		
SN54S287(J, W)	SN74S287(J, N)	1024 bits (256 W x 4 B)	three-state	42 ns	500 mW
SN54S387(J, W)	SN74S387(J, N)		open-collector		
SN54S470(J)	SN74S470(J, N)	2048 bits (256 W x 8 B)	open-collector	50 ns	550 mW
SN54S471(J)	SN74S471(J, N)		three-state		
SN54S472(J)	SN74S472(J, N)	4096 bits (512 W x 8 B)	three-state	65 ns	600 mW
SN54S473(J)	SN74S473(J, N)		open-collector		
SN54S474(J, W)	SN74S474(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S475(J, W)	SN74S475(J, N)		open-collector		

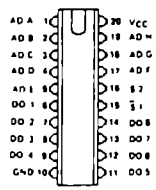
256 BITS (32 WORDS BY 8 BITS) 'S188, 'S288



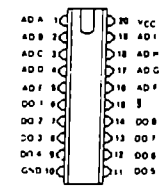
1024 BITS (256 WORDS BY 4 BITS) 'S287, 'S387



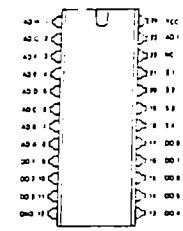
2048 BITS (256 WORDS BY 8 BITS) 'S470, 'S471



4096 BITS (512 WORDS BY 8 BITS) 'S472, 'S473



4096 BITS (512 WORDS BY 8 BITS) 'S474, 'S475



Pin assignments for all of these memories are the same for all packages

description

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in one millisecond or less. These PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit 20-pin PROM's can be used to significantly improve system density for fixed memories as all are offered in a dual-in-line package having pin-row spacings of 0.300 inch.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,976.

description (continued)

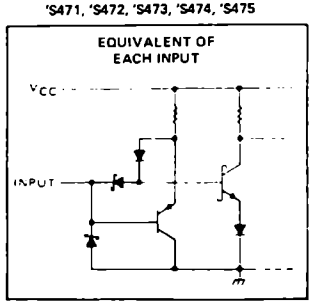
Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387, are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

Active level(s) at the chip-select input(s) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off.

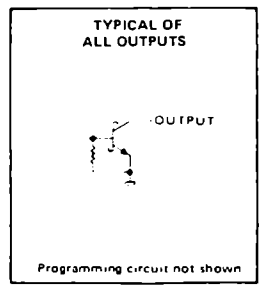
The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs

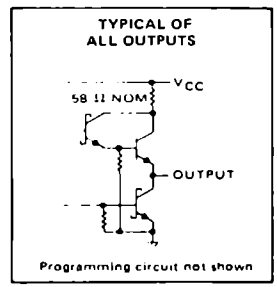
'S188, 'S287, 'S288, 'S387, 'S470, 'S471, 'S472, 'S473, 'S474, 'S475



'S188, 'S387, 'S470, 'S473, 'S475



'S287, 'S288, 'S471, 'S472, 'S474



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54S' Circuits	−55°C to 125°C
	SN74S' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

recommended conditions for programming

		SN54S', SN74S'			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.75	V
	Program pulse	10	10.5	11†	
Input voltage	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse Y (see Figure 2 and Note 3)		0.9	1	10	ms
Programming duty cycle			25	35	%
Free-air temperature		0		55	°C

†Absolute maximum ratings.

NOTES: 1. Voltage values are with respect to network ground terminal. The supply-voltage rating does not apply during programming.
2. The 'S188, 'S288, 'S470, 'S471, 'S472, 'S473, 'S474, and 'S475 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
3. Programming is guaranteed if the pulse applied is 0.9 ms long.

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step-by-step programming procedure

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9 kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current out of the programming output supply during programming is 150 mA.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 10 μs and 1 ms after V_{CC} has reached its 10.5-V level. See programming sequence of Figure 2.
7. After the X pulse time (1 ms) is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within 10 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.

NOTE: Only one programming attempt per bit is recommended.

LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION
FIGURE 1

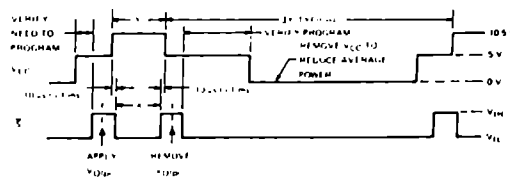

FIGURE 2–VOLTAGE WAVEFORMS FOR PROGRAMMING

recommended operating conditions

		'287, 'S471			'S288			'S472, 'S474			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	Series 54S			−2			−2			−2	mA
	Series 74S			−6.5			−6.5			−6.5	
Low-level output current, I_{OL}				16			20			12	mA
Operating free-air temperature, T_A	Series 54S	−55		125♦	−55		125	−55		125	°C
	Series 74S	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54S'			SN74S'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX		2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX				0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,				50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,				−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4		'S287		100	135		100	135	mA
				'S288		80	110		80	110	
				'S471		110	155		110	155	
				'S472, 'S474		120	155		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{S})}$ (ns) Access time from chip select (enable time)		t_{PXZ} (ns) Disable time from high or low level	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MAX
SN54S287	C_L = 30 pF for $t_{a(ad)}$ and $t_{a(\overline{S})}$; 5 pF for t_{PXZ}; R_L = 300 Ω; See Figure 4	42	75	15	40	12	40
SN74S287		42	65	15	35	12	35
SN54S288		25	50	12	30	8	30
SN74S288		25	40	12	25	8	20
SN54S471		50	80	20	40	15	35
SN74S471		50	70	20	35	15	30
SN54S472, SN54S474		55	85	20	45	15	40
SN74S472, SN74S474		55	75	20	40	15	35

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
♦An SN54S287 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 4: The typical values of I_{CC} shown are with all outputs low.

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recommended operating conditions

		'S188			'S387, 'S470			'S473, 'S475			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}				20			16			12	mA
Operating free-air temperature, T_A	Series 54S	−55		125	−55		125♦	−55		125	°C
	Series 74S	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

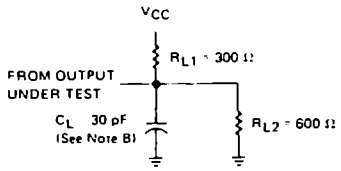
	PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50	µA
			V_{OH} = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250	µA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	'S188		80	110	mA
			'S387		100	135	
			'S470		110	155	
			'S473, 'S475		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

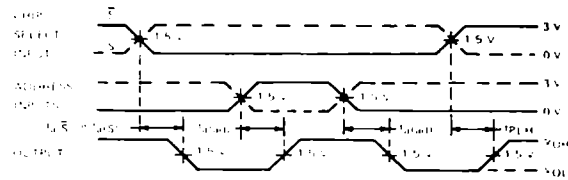
TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address		$t_{a(\overline{S})}$ (ns) Access time from chip select (enable time)		t_{PLH} (ns) Propagation delay time, low-to-high-level output from chip select (disable time)	
		TYP‡	MAX	TYP‡	MAX	TYP‡	MAX
SN54S188	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 3	25	50	12	30	12	30
SN74S188		25	40	12	25	12	25
SN54S387		42	75	15	40	15	40
SN74S387		42	65	15	35	15	35
SN54S470		50	80	20	40	15	35
SN74S470		50	70	20	35	15	30
SN54S473, SN54S475		55	85	20	45	15	40
SN74S473, SN74S475		65	75	20	40	15	35

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦An SN54S387 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 4: The typical values of I_{CC} shown are with all outputs low.

PARAMETER MEASUREMENT INFORMATION



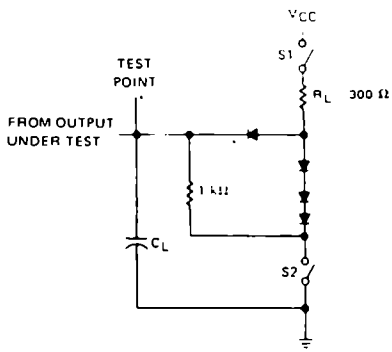
LOAD CIRCUIT



VOLTAGE WAVEFORMS

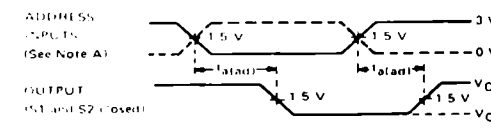
NOTES:
A. The input pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, PRR ≤ 1 MHz, $t_r \leq 2.5$ ns, and $t_f \leq 2.5$ ns.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 3 – SWITCHING TIMES OF 'S188, 'S470, 'S387, 'S473, AND 'S475

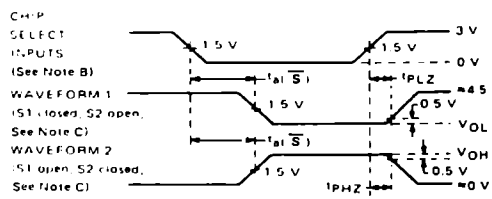


CL includes probe and jig capacitance
All diodes are 1N3064

LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



tPXZ = tPHZ or tPLZ

ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP SELECT VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the chip select input(s) is(are) low.
B. When measuring access and disable times from chip select input(s), the address inputs are steady state.
C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

FIGURE 4 – SWITCHING TIMES OF 'S287, 'S288, 'S471, 'S472, AND 'S474

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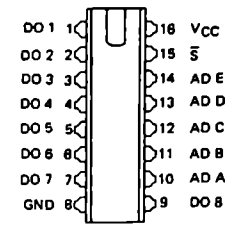
SERIES 54/74, 54S/74S
READ-ONLY MEMORIES

BULLETIN NO. DL-S 7512259, MAY 1975

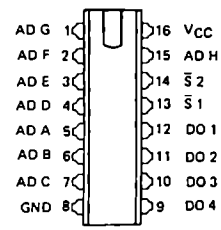
- Mask-Programmed Memories That Can Replace PROMs
- Full On-Chip Decoding and Fast Chip Select(s) Simplify System Decoding
- All Schottky-Clamped ROMs Offer
  - —Choice of 3-State or Open-Collector Outputs
  - —P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Applications Include:
  - —Microprogramming Firmware/Firmware Loaders
  - —Code Converters/Character Generators
  - —Translators/Emulators
  - —Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		TYPE OF	BIT SIZE	TYPICAL ACCESS TIMES	
−55°C to 125°C	0°C to 70°C	OUTPUT(S)	(ORGANIZATION)	CHIP-SELECT	ADDRESS
SN5488A(J, W)	SN7488A(J, N)	Open-Collector	256 Bits (32 W x 8 B)	22 ns	26 ns
SN54187(J, W)	SN74187(J, N)	Open-Collector	1024 Bits (256 W x 4 B)	20 ns	40 ns
SN54S270(J)	SN74S270(J, N)	Open-Collector	2048 Bits (512 W x 4 B)	15 ns	45 ns
SN54S370(J)	SN74S370(J, N)	3-State			
SN54S271(J)	SN74S271(J, N)	Open-Collector	2048 Bits (256 W x 8 B)	15 ns	45 ns
SN54S371(J)	SN74S371(J, N)	3-State			

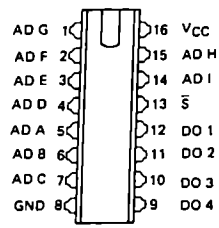
256 BITS (32 WORDS BY 8 BITS)
'88A



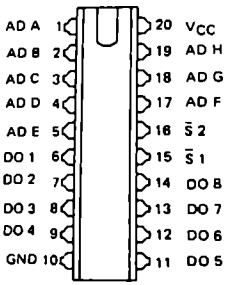
1024 BITS (256 WORDS BY 4 BITS)
'187



2048 BITS (512 WORDS BY 4 BITS)
'S270, 'S370



2048 BITS (256 WORDS BY 8 BITS)
'S271, 'S371



Pin assignments for all of these memories are the same for all packages.

description

These monolithic TTL custom-programmed read-only memories (ROMs) are particularly attractive for applications requiring medium to large quantities of the same bit pattern. Plug-in replacements can be obtained for most of the popular TTL PROMs.

The high-complexity 2048-bit ROMs can be used to significantly improve system bit density for fixed memory as all are offered in compact 16- or 20-pin dual-in-line packages having pin-row spacings of 0.300-inch.

The Schottky-clamped versions offer considerable flexibility for upgrading existing designs or improving new designs as they feature improved performance; plus, they offer low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

Data from a sequenced deck of data cards punched according to the specified format are permanently programmed by the factory into the monolithic structure for all bit locations. Upon receipt of the order, Texas Instruments will assign a special identifying number for each pattern programmed according to the order. The completed devices will be marked with the appropriate TI special device number. It is important that the customer specify not only the output levels desired at all bit locations, but also the other information requested under ordering instructions.

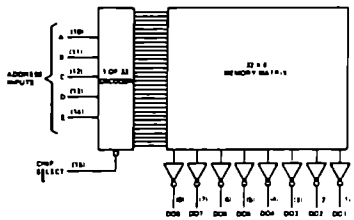
The three-state outputs offer the convenience of an open-collector output with the speed of a totem-pole output; they can be bus-connected to other similar outputs yet they retain the fast rise time characteristic of the TTL totem-pole output. The open-collector outputs offer the capability of direct interface with a data line having a passive pull-up.

Word-addressing is accomplished in straight positive-logic binary and the memory may be read when all $\overline{S}$ inputs are low. A high at any $\overline{S}$ input causes the outputs to be off.

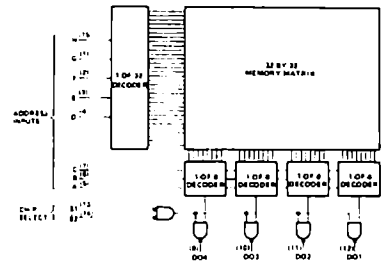
Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

functional block diagrams

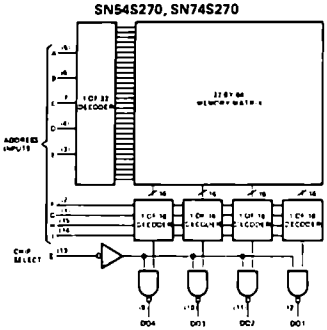
SN5488A, SN7488A



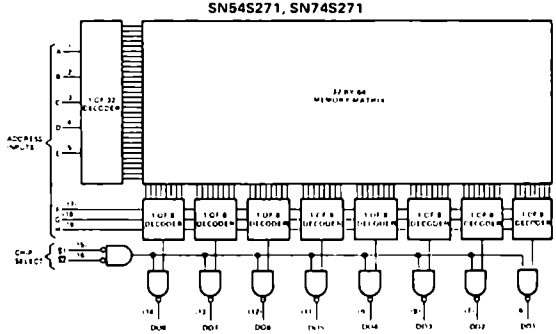
SN54187, SN74187



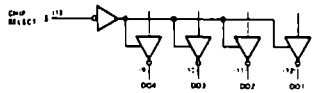
SN54S270, SN74S270



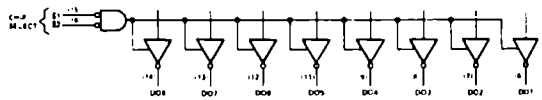
SN54S271, SN74S271



SN54S370, SN74S730
Same as SN54S270, SN74S270 except outputs are as shown below:



SN54S371, SN74S371
Same as SN54S271, SN74S271 except outputs are as shown below:



word addressing

'88A

WORD ADDRESS TABLE

WORD	INPUTS				
	E	D	C	B	A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
	Words 9 thru 26 omitted				
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

'187, 'S271, 'S371

WORD ADDRESS TABLE

WORD	INPUTS							
	H	G	F	E	D	C	B	A
0	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	H	L
3	L	L	L	L	L	L	H	H
4	L	L	L	L	L	H	L	L
5	L	L	L	L	L	H	L	H
6	L	L	L	L	L	H	H	L
7	L	L	L	L	L	H	H	H
8	L	L	L	L	H	L	L	L
	Words 9 thru 250 omitted							
251	H	H	H	H	H	L	H	H
252	H	H	H	H	H	H	L	L
253	H	H	H	H	H	H	L	H
254	H	H	H	H	H	H	H	L
255	H	H	H	H	H	H	H	H

'S270, 'S370

WORD ADDRESS TABLE

WORD	INPUTS									
	I	H	G	F	E	D	C	B	A	
0	L	L	L	L	L	L	L	L	L	
1	L	L	L	L	L	L	L	L	H	
2	L	L	L	L	L	L	L	H	L	
3	L	L	L	L	L	L	L	H	H	
4	L	L	L	L	L	L	H	L	L	
5	L	L	L	L	L	L	H	L	H	
6	L	L	L	L	L	L	H	H	L	
7	L	L	L	L	L	L	H	H	H	
8	L	L	L	L	L	H	L	L	L	
	Words 9 thru 506 omitted									
507	H	H	H	H	H	H	L	H	H	
508	H	H	H	H	H	H	H	L	L	
509	H	H	H	H	H	H	H	L	H	
510	H	H	H	H	H	H	H	H	L	
511	H	H	H	H	H	H	H	H	H	

Word selection is accomplished in a conventional positive-logic binary code with the A address input being the least-significant bit progressing alphabetically through the address inputs to the most-significant bit.

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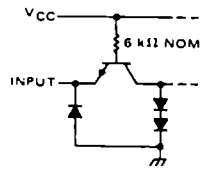
schematics of inputs and outputs

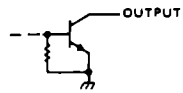
'88A, '187

EQUIVALENT OF EACH INPUT



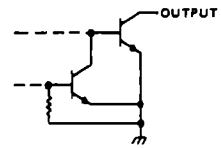
'88A

TYPICAL OF ALL OUTPUTS



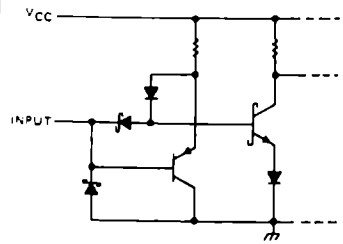
'187

TYPICAL OF ALL OUTPUTS



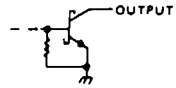
'S270, 'S271, 'S370, 'S371

EQUIVALENT OF EACH INPUT



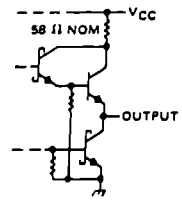
'S270, 'S271

TYPICAL OF ALL OUTPUTS



'S370, 'S371

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54', SN54S' Circuits (see Note 2)	−55°C to 125°C
	SN74', SN74S' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54187 in the W package operating at free-air temperatures above 111°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 46°C/W.

recommended operating conditions

	SN5488A			SN7488A			SN54187			SN74187			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}			12			12			16			16	mA
Operating free-air temperature, T_A (see Note 2)	−55		125	0		70	−55		125	0		70	C

NOTE 2: An SN54187 in the W package operating at free-air temperatures above 111 C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 46 C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'88A			'187			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	V_{OH} = 5.5 V			40			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA		0.2	0.4			0.4	V
			I_{OL} = 16 mA						0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			25			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1			−1	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		64	80		92	130	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, V_O = 5 V, f = 1 MHz			6.5			6.5		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 3: With outputs open and $\overline{CS}$ input(s) grounded, I_{CC} is measured first by selecting a word that contains the maximum number of programmed high-level outputs, then by selecting a word that contains the maximum number of programmed low-level outputs.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'88A		'187		UNIT
			TYP	MAX	TYP	MAX	
$t_{a(ad)}$	Access time from address	C_L = 30 pF,	26	45	40	60	ns
$t_{a(\overline{S})}$	Access time from chip select (enable time)	R_{L1} = 400 Ω ('88A) 300 Ω ('187)	22	35	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select (disable time)	R_{L2} = 600 Ω, See Figure 1	22	35	20	30	ns

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recommended operating conditions

	SN54S270 SN54S271			SN74S270 SN74S271			SN54S370 SN54S371			SN74S370 SN74S371			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5							V
High-level output current, I_{OH}									−2			−6.5	mA
Low-level output current, I_{OL}			16			16			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'S270, 'S271			'S370, 'S371			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OH} = MAX				2.4			V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50				μA
			V_{OH} = 5.5 V			100				μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V							50	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V							−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX					−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 4		105	155		105	155	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, V_O = 5 V, f = 1 MHz			6.5			6.5		pF

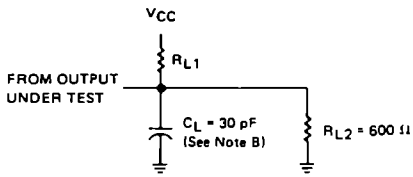
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 4: With outputs open and $\overline{CS}$ input(s) grounded, I_{CC} is measured first by selecting a word that contains the maximum number of programmed high-level outputs, then by selecting a word that contains the maximum number of programmed low-level outputs.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

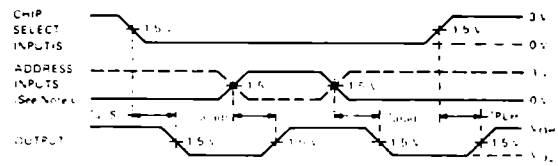
PARAMETER		TEST CONDITIONS	SN54270 SN54271		SN74270 SN74271		SN54370 SN54370		SN74370 SN74370		UNIT
			TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address	R_{L2} = 600 Ω, See Figure 1	45	95	45	70					ns
$t_{a(\overline{S})}$	Access time from chip select (enable time)		15	45	15	30					ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select (disable time)		15	40	15	25					ns
$t_{a(ad)}$	Access time from address	C_L = 30 pF, See Figure 2					45	95	45	70	ns
$t_{a(\overline{S})}$	Access time from chip select (enable time)						15	45	15	30	ns
t_{PXZ}	Disable time from high or low level	C_L = 5 pF, See Figure 2					10	40	10	25	ns

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



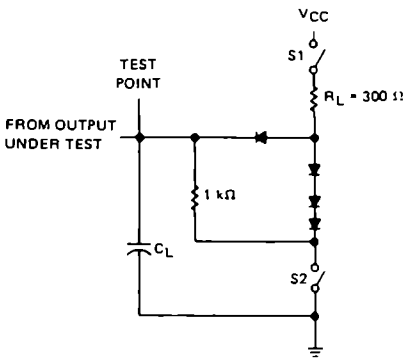
LOAD CIRCUIT



VOLTAGE WAVEFORMS

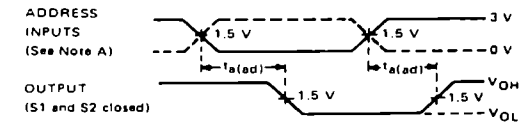
NOTES A. The input pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$. For Series 54/74, $t_r \leq 7$ ns, $t_f \leq 7$ ns; for Series 54S/74S, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 1–SWITCHING TIMES OF '88A, '187, 'S270, AND 'S271 (OPEN-COLLECTOR OUTPUTS)

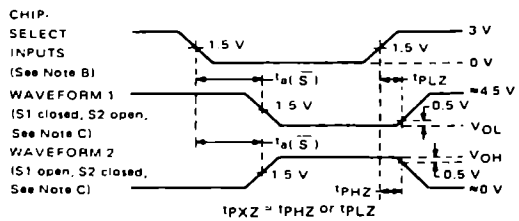


C_L includes probe and jig capacitance.
All diodes are 1N3064

LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS
VOLTAGE WAVEFORMS



$t_{PXZ} = t_{PHZ}$ or t_{PLZ}

ACCESS (ENABLE) TIME FROM CHIP SELECT
VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the chip-select input(s) is(are) low.
B. When measuring access and disable times from chip-select input(s) the address inputs are steady-state.
C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.6$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

FIGURE 2–SWITCHING TIMES OF 'S370 AND 'S371 (3-STATE OUTPUTS)

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ORDERING INSTRUCTIONS

Programming instructions for these read-only memories are solicited in the form of a sequenced deck of standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table for the requested part. This function table, showing output conditions for each of the words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the words specified and describes the levels at the outputs for each of those words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

The following information will be furnished to the customer by Texas Instruments:

a) TI part number
b) TI sales order number
c) Date received.

'88A DATA CARD FORMAT (32 CARDS)

Column	
1-2	Punch a right-justified integer representing the positive-logic binary input address (00-31) for the word described on the card.
3-4	Blank
5	Punch "H" or "L" for output Y8. H = high-voltage-level output, L = low-voltage-level output
6-9	Blank
10	Punch "H" or "L" for output DO 7.
11-14	Blank
15	Punch "H" or "L" for output DO 6.
16-19	Blank
20	Punch "H" or "L" for output DO 5.
21-24	Blank
25	Punch "H" or "L" for output DO 4.
26-29	Blank
30	Punch "H" or "L" for output DO 3.
31-34	Blank
35	Punch "H" or "L" for output DO 2.
36-39	Blank
40	Punch "H" or "L" for output DO 1.
41-49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "SN"
62-66	Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.
67-68	Blank
69-80	Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

'187 DATA CARD FORMAT (32 CARDS)

Column	
1- 3	Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.
8- 9	Blank

ORDERING INSTRUCTIONS

10-13	Punch "H", "L", or "X" for bits four, three, two, and one (outputs DO 4, DO 3, DO 2 and DO 1 in that order) for the first set of outputs specified on the card. H = high-voltage-level output, L = low-voltage-level output, X = output level irrelevant.
14	Blank
15-18	Punch "H", "L", or "X" for the second set of outputs.
19	Blank
20-23	Punch "H", "L", or "X" for the third set of outputs.
24	Blank
25-28	Punch "H" "L", or "X" for the fourth set of outputs.
29	Blank
30-33	Punch "H", "L", or "X" for the fifth set of outputs.
34	Blank
35-38	Punch "H", "L", or "X" for the sixth set of outputs.
39	Blank
40-43	Punch "H", "L", or "X" for the seventh set of outputs.
44	Blank
45-48	Punch "H", "L", or "X" for the eighth set of outputs.
49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "SN"
62-66	Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.
67-68	Blank
69-80	Preferably these columns should be punched to reflect the customer's part or specification control number. This information is not essential.

'S270, 'S370 DATA CARD FORMAT (64 CARDS)

Column	
1-3	Punch a right-justified integer representing the binary input address (000-504) for the first set of outputs described on the card.
4	Punch a "—" (Minus sign)
5-7	Punch a right-justified integer representing the binary input address (007-511) for the last set of outputs described on the card.
8-80	Same as the '187 data card format.

'S271, 'S371 DATA CARD FORMAT (64 CARDS)

Column	
1-3	Punch a right-justified integer representing the binary input address (000-252) for the first set of outputs described on the card.
4	Punch a "-" (Minus sign)
5-7	Punch a right-justified integer representing the binary input address (003-255) for the last set of outputs described on the card.
8-9	Blank
10-17	Punch "H", "L", or "X" for bits eight, seven, six, five, four, three, two, and one (outputs DO 8, DO 7, DO 6, DO 5, DO 4, DO 3, DO 2, and DO 1 in that order) for the first set of outputs specified on the card. H = high-voltage-level output, L = low-voltage-level output, X = output level irrelevant.
18	Blank
19-26	Punch "H", "L", or "X" for the second set of outputs
27	Blank
28-35	Punch "H", "L", or "X" for the third set of outputs.
36	Blank
37-44	Punch "H", "L", or "X" for the fourth set of outputs.
45-49	Blank
50-80	Same as the '187 data card format.

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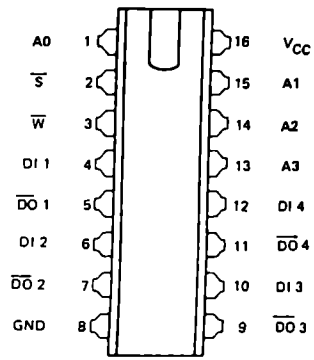
64-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

SEPTEMBER 1976

- Static Fully Decoded Ram's Organized as 16 Words of Four Bits Each
- Schottky-Clamped for High Speed:
  - Read Cycle Time . . . 25 ns Typical
  - Write Cycle Time . . . 25 ns Typical
- Choice of Three-State or Open-Collector Outputs
- Compatible with Most TTL and I^2L Circuits
- Chip-Select Input Simplifies External Decoding

SN54S189, SN54S289 . . . J OR W PACKAGE
SN74S189, SN74S289 . . . J OR N PACKAGE
(TOP VIEW)



Pin assignments are same for all packages.

description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four bits each. They are fully decoded and feature a chip-select input to simplify decoding required to achieve expanded system organization. The memories feature p-n-p input transistors that reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a Series 54S/74S standard load factor. The chip-select circuitry is implemented with minimal delay times to compensate for added system decoding.

write cycle

The information applied at the data input is written into the selected location when the chip-select input and the write-enable input are low. While the write-enable input is low, the 'S189 output is in the high-impedance state and the 'S289 output is off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

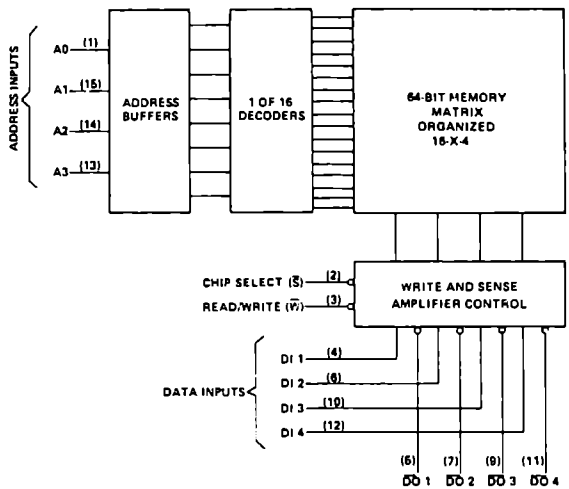
The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the 'S189 output will be in the high-impedance state and the 'S289 output will be off.

FUNCTION TABLE

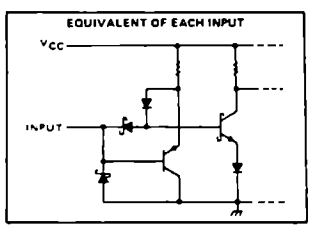
FUNCTION	INPUTS		'S189	'S289
	CHIP SELECT	WRITE ENABLE	OUTPUT	OUTPUT
Write	L	L	High Impedance	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered
Inhibit	H	X	High Impedance	Off

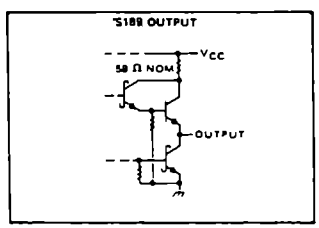
H = high level, L = low level, X = irrelevant

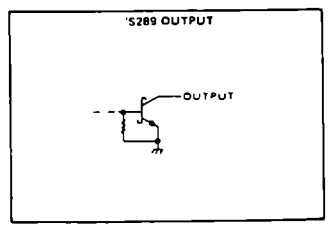
functional block diagram



schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		5.5 V
Off-State output voltage		5.5 V
Operating free-air temperature range:	SN54S' Circuits	−55°C to 125°C
	SN74S' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

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recommended operating conditions

		SN54S189			SN54S289			SN74S189			SN74S289			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}							5.5						5.5	V
High-level output current, I_{OH}				−2						−6.5				mA
Low-level output current, I_{OL}				16			16			16			16	mA
Width of write pulse (write enable low), $t_{w(wr)}$		25			25			25			25			ns
Setup time	Address before write pulse, $t_{su(da)}$	0↓			0↓			0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	25↑			25↑			25↑			25↑			
	Chip-select before end of write pulse, $t_{su(\overline{S})}$	25↑			25↑			25↑			25↑			
Hold time	Address after write pulse, $t_{h(ad)}$	0↑			0↑			0↑			0↑			ns
	Data after write pulse, $t_{h(da)}$	0↑			0↑			0↑			0↑			
	Chip-select after write pulse, $t_{h(\overline{S})}$	0↑			0↑			0↑			0↑			
Operating free-air temperature, T_A		−55		125	−55		125	0		70	0		70	°C

†The arrow indicates the transition of the write-enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (otherwise noted)

PARAMETER		TEST CONDITIONS†		'189			'289			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	SN54S'	2.4	3.4					V
			SN74S'	2.4	3.2					
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O=2.4 V						40	μA
			V_O=5.5 V						100	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA	SN54S'		0.35	0.5		0.35	40	V
			SN74S'		0.35	0.45		0.35	100	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 2.4 V				50				μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OL} = 0.4 V				−50				μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100				mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			75	110		75	105	mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. I_{CC} is measured with the read/write and chip-select inputs grounded. All other inputs at 4.5V, and the outputs open.

'S189 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S189		SN74S189		UNIT
				TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_L = 300 Ω See Note 3	25	50	25	35	ns
$t_{a(S)}$	Access time from chip select (enable time)			12	25	12	17	ns
t_{SR}	Sense recovery time			22	40	22	35	ns
t_{PXZ}	Disable time from high or low level	from $\overline{S}$	C_L = 5 pF, R_L = 300 Ω, See Note 3	12	25	12	17	ns
		from $\overline{W}$		12	30	12	25	

'S289 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S289		SN74S289		UNIT
				TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Note 3	25	50	25	35	ns
$t_{a(S)}$	Access time from chip select (enable time)			12	25	12	17	ns
t_{SR}	Sense recovery time			22	40	22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	from $\overline{S}$		12	25	12	17	ns
		from $\overline{W}$		12	30	12	25	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C

NOTES: 3. Load circuit and voltage wave forms are shown in Appendix A, page 44.

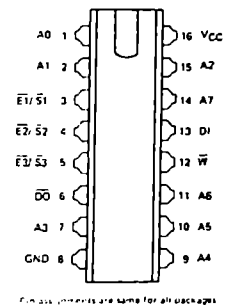
256-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

NOVEMBER 1976

- Static Fully Decoded RAM's Organized as 256 Words of One Bit Each
- Schottky-Clamped for High Performance
- Choice of Three-State or Open-Collector Outputs
- Compatible with Most TTL and I^2L Circuits
- Chip-Enable/Select Inputs Simplify External Decoding
- Typical Performance:

TYPES	READ ACCESS TIME	POWER DISS.
SN74S200A/'S300A	30 ns	500 mW
SN54S200A/'S300A	30 ns	500 mW
SN74LS200A/'LS300A	35 ns	275 mW
SN54LS200A/'LS300A	35 ns	275 mW
SN74LS202/'LS302	35 ns	275 mW
SN54LS202/'LS302	35 ns	275 mW
S202/'LS302 POWER DOWN	(65 ns enable)	100 mW

SN54LS200A, SN54LS300A
SN54LS202, SN54LS302
SN54S200A, SN54S300A . . J OR W PACKAGE
SN74LS200A, SN74LS300A
SN74LS202, SN74LS302
SN74S200A, SN74S300A . . J OR N PACKAGE
(TOP VIEW)



Pin assignments are same for all packages

$\overline{E1}$, $\overline{E2}$, $\overline{E3}$, = Chip-Enable for 'LS202, 'LS302
$\overline{S1}$, $\overline{S2}$, $\overline{S3}$, = Chip-Select for 'LS200A, 'LS300, 'S200A, 'S300A.

description

These 256-bit active-element memories are monolithic transistor-transistor logic (TTL) arrays organized as 256 words of one bit. They are fully decoded and have three chip-enable/select inputs to simplify decoding required to achieve expanded system organizations. When the 'LS202/'LS302 is disabled, all read and write functions are in a power-down mode, that is, turned off.

write cycle

The information applied at the data input is written into the selected location when the three chip-enable/select inputs and the write-enable input are low. While the write-enable input is low, the 'S200A, 'LS200A and 'LS202 outputs are in the high-impendance state and the 'S300A, 'LS300A and 'LS302 outputs are off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three chip-enable/select inputs are low. When any one of the chip-enable/select inpts are high, the 'S200A, 'LS200A, or 'LS202 outputs will be in the high-impedance state, the S300A, LS300A, or LS302 outputs will be off, and the 'LS202 or 'LS302 will be in a power-down mode.

DESIGN GOAL
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

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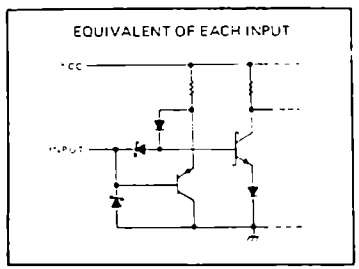
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

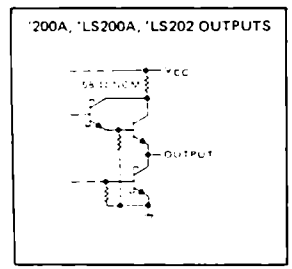
FUNCTION TABLE

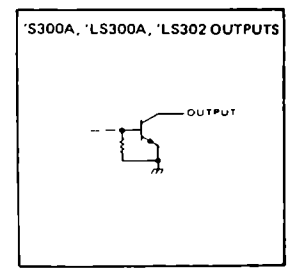
FUNCTION	INPUTS		'S200A 'LS200A 'LS202 OUTPUT ($\overline{DO}$)	'S300A 'LS300A 'LS302 OUTPUT ($\overline{DO}$)
	CHIP ENABLE ($\overline{E}_i$) OR SELECT ($\overline{S}_i$)	WRITE ENABLE ($\overline{W}$)		
Write	L	L	High Impedance	Off
Read	L	H	Complement of Date Entered	Complement of Data Entered
Inhibit	H	X	High Impedance	Off

H = high level, L = low level, X = irrelevant. †For chip enable/select: L = all $\overline{E}_i$ or $\overline{S}_i$ inputs low, H = one or more $\overline{E}_i$ or $\overline{S}_i$ inputs high

schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-State output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' and SN54LS' Circuits (see Note 2) . . . . . −55°C to 125°C
SN74S' and SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54S200A or SN54S300A in the W package operating at free-air temperatures above 104°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 38° C/W.

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recommended operating conditions

		SN54S200A			SN54S300A			SN74S200A			SN74S300A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}							5.5						5.5	V
High-level output current, I_{OH}				−5.2						−10.3				mA
Low-level output current, I_{OL}				16			16			16			16	mA
Width of write pulse (write enable low), $t_{w(wr)}$		40			50			30			40			ns
Setup time	Address before write pulse, $t_{su(ad)}$	0↓			0↓			0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	40↑			50↑			30↑			40↑			
	Chip-select before end of write pulse, $t_{su(\bar{S})}$	40↑			50↑			30↑			40↑			
Hold time	Address after write pulse, $t_{h(ad)}$	5↑			5↑			5↑			5↑			ns
	Data after write pulse, $t_{h(da)}$	5↑			5↑			5↑			5↑			
	Chip-select after write pulse, $t_{h(\bar{S})}$	5↑			5↑			5↑			5↑			
Operating free-air temperature, T_A (See Note 2)		−55		125	−55		125	0		70	0		70	°C

recommended operating conditions

		SN54LS200A SN54LS300A			SN74LS200A SN74LS300A			SN54LS202 SN54LS302			SN74LS202 SN74LS302			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	'LS300A, 'LS302			5.5			5.5			5.5			5.5	V
High-level output current, I_{OH}	'LS200A, 'LS202			−2			−2.6			−2			−2.6	mA
Low-level output current, I_{OL}				16			16			16			16	mA
Width of write pulse (write enable low), $t_{w(wr)}$		50			35			15			15			ns
Setup time	Address before write pulse, $t_{su(ad)}$	20↓			15↓			0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	40↑			30↑			15↑			15↑			
	Chip enable before end of write pulse, $t_{su(\bar{E})}$, $t_{su(\bar{S})}$	50↑			40↑			35↑			35↑			
Hold time	Address after write pulse, $t_{h(ad)}$	10↑			0↑			−5↑			−5↑			ns
	Data after write pulse, $t_{h(da)}$	10↑			0↑			−5↑			−5↑			
	Chip-enable after write pulse, $t_{h(\bar{E})}$, $t_{su(\bar{S})}$	0↑			0↑			−5↑			−5↑			
Operating free-air temperature, T_A		−55		125	0		70	−55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54S200A or SN54S300A in the W Package operating at free-air temperatures above 104°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 38° C/W.

electrical characteristics over recommended operating free-air temperature range (otherwise noted)

PARAMETER		TEST CONDITIONS†			'S200A			'S300A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX		2.4						V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX	SN54S'			0.5			0.5	V
				SN74S'			0.45			0.45	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V,	V_O=2.4 V						50	μA
				V_O=5.5 V						100	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 2.4 V				50				μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OL} = 0.5 V				−50				μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−100				mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3	T_A=−55°C			143			143	mA
				T_A=0°C		100	135		100	135	
				T_A=70°C			124			124	
				T_A=125°C			117			117	

electrical characteristics over recommended operating free-air temperature range (otherwise noted)

PARAMETER		TEST CONDITIONS†			'LS200A 'LS202			'LS300A 'LS302			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX		2.4						V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX	SN54S'			0.5			0.5	V
				SN74S'			0.45			0.45	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V,	V_O=2.4 V						30	μA
				V_O=5.5 V						100	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 2.4 V				30				μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OL} = 0.5 V				−30				
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−20		−100				mA
I_{CC}	Supply current – Power up	V_{CC} = MAX,	See Note 3			55	70		55	70	mA
I_{CC}	Supply current – Power down	V_{CC} = MAX,	CE = 2.4 V	'LS202		20			20		mA
				'LS302							

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.
NOTE: 3. I_{CC} is measured with all inputs grounded and the output open.

'S200A, 'LS200A switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S200A		SN74S200A		SN54LS200A		SN74LS200A		UNIT
				TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_L = 400 Ω, See Note 4	30	60	30	40	35	55	35	45	ns
$t_{a(S)}$	Access time from chip select (select time)			15	40	15	30	15	30	15	25	ns
t_{SR}	Sense recovery time				50		40		55		45	ns
t_{PXZ}	Disable time from high or low level	From $\overline{S}$	C_L = 5 pF, R_L = 400 Ω, See Note 4	15	40	15	30	15	30	15	25	ns
		From $\overline{W}$		20	45	20	35	20	40	20	30	

'S300A and 'LS300A switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S300A		SN74S300A		SN74LS300A		SN74LS300A		UNIT
				TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Note 4	30	65	30	45	35	55	35	45	ns
$t_{a(S)}$	Access time from chip enable (enable time)			15	40	15	30	15	30	15	25	ns
t_{SR}	Sense recovery time				50		40		55		45	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	From $\overline{S}$		15	35	15	30	15	30	15	25	ns
		From $\overline{W}$		20	45	20	35	20	40	20	30	

'LS202 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54LS202		SN74LS202		UNIT
				TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_L = 400 Ω, See Note 4	35		35		ns
t_a ($\overline{E}$)	Access time from chip enable (enable time)			45		45		ns
t_{SR}	Sense recovery time			20		20		ns
t_{PXZ}	Disable time from high or low level	From $\overline{E}$	C_L = 5 pF, R_{L1} = 400 Ω, See Note 4	20		20		ns
		From $\overline{W}$		20		20		
t_{EPD}	Chip power-down time		See Figure 1	65		65		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE: 4. Load circuit and voltage waveforms are shown in Appendix A, page 44.

'LS302 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54LS302 TYP†	SN54LS302 MAX	SN74LS302 TYP‡	SN74LS302 MAX	UNIT
$t_{a(ad)}$	Access time from address		C_L = 15 pF, R_{L1} = 400 Ω, R_{L2} = 600 Ω, See Note 5	35		35		ns
$t_a(\overline{E})$	Access time from chip enable (enable time)			45		45		ns
t_{SR}	Sense recovery time			20		20		ns
t_{PLH}	Propagation delay time, low-to-high level output (disable time)	From $\overline{CE}$		20		20		ns
		From $\overline{W}$		20		20		
t_{EPD}	Chip power-down time (I_{CC} ≤ 38.5 mA)		See Figure 1	65		65		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE: 5. Load circuit and voltage waveforms are shown in Appendix A, page 44.

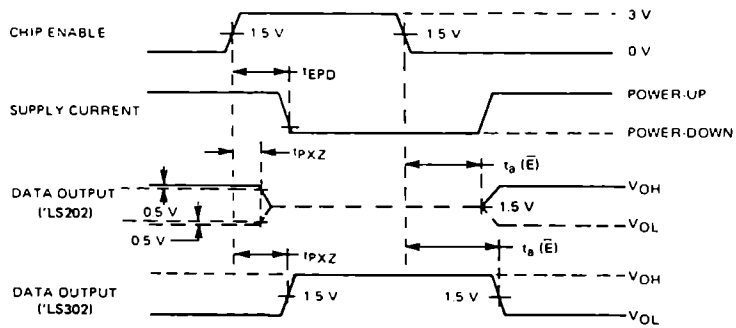

FIGURE 1. POWER-DOWN WAVEFORMS

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1024-BIT HIGH-PERFORMANCE RANDOM-ACCESS MEMORIES

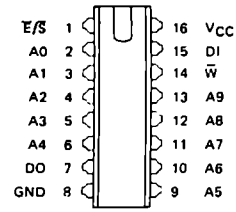
DECEMBER 1976

- Static Fully Decoded RAM's Organized 1024 Words of One Bit Each
- Schottky-Clamped for High Performance
- Choice of Three-State or Open-Collector Outputs
- Compatible with Most TTL and I^2L Circuits
- Chip-Enable/Select Inputs Simplify External Decoding
- Typical Performance

TYPES	READ ACCESS TIMES	POWER DISS
SN74S214A/'S314A	30 ns	550 mW
SN74S214/'S314	40 ns	550 mW
SN54S214/'S314	40 ns	550 mW
SN74LS214/'LS314	75 ns	200 mW
SN54LS214/'LS314	75 ns	200 mW
SN74LS215/'LS315	75 ns	200 mW
SN54LS215/'LS315	75 ns	200 mW
'LS215/'LS315 POWER DOWN		100 mW

SN54LS214, SN64LS314
SN54LS215, SN54LS315
SN54S214, SN54S314 . . . J PACKAGE

SN74LS214, SN74LS314
SN74LS215, SN74LS315
SN74S214A, SN74S314A
SN74S214, SN74S314 . . . J OR N PACKAGE
(TOP VIEW)



Pin assignments are same for all packages.
$\overline{E}$ = Chip-Enable for 'LS215, 'LS315
$\overline{S}$ = Chip-Select for 'LS214, 'LS314, 'S214, 'S314 'S314A, 'S214A

description

These 1024-bit active-element memories are monolithic transistor-transistor logic (TTL) arrays organized as 1024 words of one bit. They are fully decoded and have a chip-enable or chip-select input to simplify decoding required to achieve expanded system organizations. When the 'LS215/'LS315 is disabled, all read and write functions are in a power-down mode, that is, turned off.

write cycle

The information applied at the data input is written into the selected location when the chip-enable/select input and the write-enable input are low. While the write-enable input is low, the 'S214A, 'S214, 'LS214, and 'LS215 outputs are in the high-impedance state and the 'S314A, 'S314, 'LS314 and 'LS315 outputs are off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

The stored information is available at the output when the write-enable input is high and the chip-enable/select input is low. When the chip-enable/select Input is high, the 'S214A, 'S214, 'LS214, or 'LS215 output will be in the high-impedance state, the 'S314A, S314, LS314, or LS315 output will be off, and the 'LS215 or 'LS315 will be in a power-down mode.

DESIGN GOAL

This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

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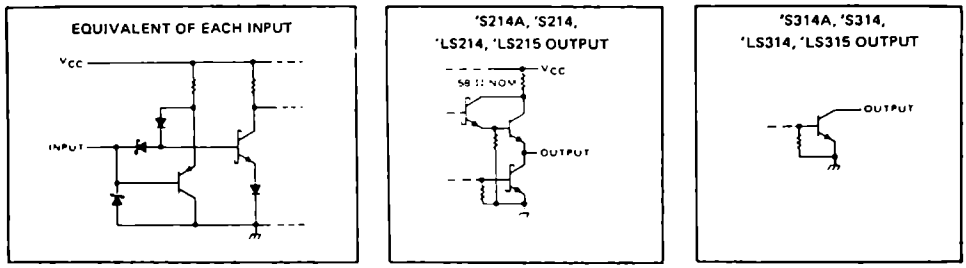
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U. S. Patent Number 3,463,975.

FUNCTION TABLE

FUNCTION	INPUTS		'S214A 'S214 'LS214 'LS215 OUTPUT (DO)	'S314A 'S314 'LS314 'LS315 OUTPUT (DO)
	CHIP ENABLE ($\overline{E}$) OR SELECT ($\overline{S}$)	WRITE ENABLE ($\overline{W}$)		
Write	L	L	High Impedance	Off
Read	L	H	Stored Data	Stored Data
Inhibit	H	X	High Impedance	Off

H = high level, L = low level, X = irrelevant

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-State output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' and SN54LS' Circuits . . . . . −55°C to 125°C
SN74S' and SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE: 1. Voltage values are with respect to network ground terminal.

'S214A, 'S214 recommended operating conditions

		SN54S214			SN74S214A			SN74S214			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output current, I_{OH}				−5.2			−10.3			−10.3	mA
Low-level output current, I_{OL}				16			16			16	mA
Width of write pulse (write enable low), $t_{w(wr)}$		55			35			50			ns
Setup time	Address before write pulse, $t_{su(ad)}$	15↓			5↓			15↓			ns
	Data before end of write pulse, $t_{su(da)}$	60↑			40↑			65↑			
	Chip select before end of write pulse, $t_{su(\overline{S})}$	60↑			40↑			65↑			
Hold time	Address after write pulse, $t_{h(ad)}$	5↑			5↑			5↑			ns
	Data after write pulse, $t_{h(da)}$	5↑			5↑			5↑			
	Chip select after write pulse, $t_{h(\overline{S})}$	5↑			5↑			5↑			
Operating free-air temperature, T_A		−55		125	0		70	0		70	°C

'S314A, 'S314 recommended operating conditions

		SN54S314			SN74S314A			SN74S314			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}				16			16			16	mA
Width of write pulse (write enable low), $t_{w(wr)}$		55			35			50			ns
Setup time	Address before write pulse, $t_{su(ad)}$	15↓			5↓			15↓			ns
	Data before end of write pulse, $t_{su(da)}$	60↑			40↑			65↑			
	Chip select before end of write pulse, $t_{su(\overline{S})}$	60↑			40↑			65↑			
Hold time	Address after write pulse, $t_{h(ad)}$	5↑			5↑			5↑			ns
	Data after write pulse, $t_{h(da)}$	5↑			5↑			5↑			
	Chip select after write pulse, $t_{h(\overline{S})}$	5↑			5↑			5↑			
Operating free-air temperature, T_A		−55		125	0		70	0		70	°C

↑↓The arrow indicates the transition from the read/write input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

NOTE: 1. Voltage values are with respect to network ground terminal.

'LS214, 'LS314, 'LS215, 'LS315 recommended operating conditions

		SN54LS214 SN54LS314			SN74LS214 SN74LS314			SN54LS215 SN54LS315			SN74LS215 SN74LS315			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	'LS314, 'LS315			5.5			5.5			5.5			5.5	V
High-level output current, I_{OH}	'LS214, 'LS215			−5.2			−5.2			−5.2			−5.2	mA
Low-level output current, I_{OL}				16			16			16			16	mA
Width of write pulse (write enable low), $t_{w(wr)}$		75			60			75			60			ns
Setup time	Address before write pulse, $t_{su(ad)}$	25↓			20↓			25↓			20↓			ns
	Data before end of write pulse, $t_{su(da)}$	95↑			75↑			95↑			75↑			
	Chip-select/enable before end of write pulse, $t_{su(\overline{E})}$, $t_{su(\overline{S})}$	95↑			75↑			95↑			75↑			
Hold time	Address after write pulse, $t_{h(ad)}$	20↑			15↑			20↑			15↑			ns
	Data after write pulse, $t_{h(da)}$	20↑			15↑			20↑			15↑			
	Chip-select/enable after write pulse $t_{h(\overline{E})}$, $t_{h(\overline{S})}$	20↑			15↑			20↑			15↑			
Operating free-air temperature, T_A		−55		125	0		70	−55		125	0		70	°C

'S214A, 'S214, 'S314A, 'S314 electrical characteristics over recommended operating free-air temperature range (otherwise noted)

PARAMETER			TEST CONDITIONS†		'S214A, 'S314A			'S214, 'S314			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	'S214A, 'S214	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	SN54S'	2.4	3.3		2.4	3.3		V
				SN74S'	2.4	2.9		2.4	2.9		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX	SN54S'			0.5			0.5	V
				SN74S'			0.45			0.45	
I_{OH}	High-level output current	'S314A, 'S314	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O=2.4 V			50			50	μA
				V_O=5.5 V			100			100	
I_{OZH}	Off-state output current, high-level voltage applied	'S214A, 'S214	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 2.4 V				50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	'S214A, 'S214	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OL} = 0.5 V				−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				25			25	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	'S214A, 'S214	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	T_A=−55°C			170			170	mA
				T_A=0°C			155			155	
				T_A=MAX			130			130	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.
NOTES: 1. Voltage values are with respect to network ground terminal.
2. I_{CC} is measured with all inputs grounded and the output open.

'LS214, 'LS314, 'LS215, 'LS315 electrical characteristics over recommended operating free-air temperature range (otherwise noted)

PARAMETER			TEST CONDITIONS†		'LS214 'LS314			'LS215 'LS315			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	'LS214, 'LS215	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5	V
I_{OH}	High-level output current	'LS314, 'LS315	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O=2.4 V			50			50	µA
				V_O=5.5 V			100			100	
I_{OZH}	Off-state output current, high-level voltage applied	'LS214, 'LS215	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 2.4 V				50			50	µA
I_{OZL}	Off-state output current, low-level voltage applied	'LS214, 'LS215	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OL} = 0.5 V				−50			−50	µA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				25			25	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5 V				−250			−250	µA
I_{OS}	Short-circuit output current§	'LS214, 'LS215	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	T_A=−55°C			75				mA
				T_A=0°C		40	65		40		
				T_A=MAX			55				
I_{CC}	Supply current — Power down	'LS215 'LS315	V_{CC} = MAX, $\overline{E}$ = 2.4 V						20		mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.
NOTE: 2. I_{CC} is measured with all inputs grounded and the output open.

'S214, 'LS214 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S214		SN74S214A		SN74S214		SN54LS214		SN74LS214		UNIT
				TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_L = 400 Ω, See Note 3	40	75	30	45	40	70	75	140	75	95	ns
$t_{a(\overline{S})}$	Access time from chip select (select time)			15	45	15	30	15	40	30	50	30	40	ns
t_{SR}	Sense recovery time			20	65	20	40	25	50	35	75	35	65	ns
t_{PXZ}	Disable time from high or low level	from $\overline{S}$	C_L = 5 pF, R_L = 400 Ω, See Note 3	20	50	15	30	20	40	30	50	30	40	ns
		from $\overline{W}$		20	45	20	30	20	40	35	60	35	60	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE: 3. Load circuit and voltage waveforms are shown in Appendix A, page 44.

'S314 and 'LS314 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S314		SN74S314A		SN74S314		SN54LS314		SN74LS314		UNIT
				TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Note 3	40	75	30	45	40	70	75	140	75	95	ns
$t_{a(\bar{S})}$	Access time from chip select (select time)			15	45	15	30	15	40	35	60	35	50	ns
t_{SR}	Sense recovery time			20	55	20	40	25	50	35	60	35	50	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	$\bar{S}$		20	50	15	30	20	40	45	70	45	60	ns
		$\bar{W}$		20	45	20	30	25	40	35	60	35	50	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C

'LS215 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TYP‡	MAX	UNIT
$t_{a(ad)}$	Access time from address		C_L = 15 pF, R_L = 400 Ω, See Note 5	75		ns
$t_{a(\bar{E})}$	Access time from chip enable (enable time)			55		ns
t_{SR}	Sense recovery time			35		ns
t_{PXZ}	Disable time from high or low level	from $\bar{E}$	C_L = 5 pF, R_{L1} = 400 Ω, See Note 3	30		ns
		from $\bar{W}$		35		
t_{EPD}	Chip power-down time		See Figure 1	65		ns

'LS315 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TYP‡	MAX	UNIT
$t_{a(ad)}$	Access time from address		C_L = 15 pF, R_{L1} = 400 Ω, R_{L2} = 600 Ω, See Note 3	75		ns
$t_{a(\bar{E})}$	Access time from chip enable (enable time)			55		ns
t_{SR}	Sense recovery time			35		ns
t_{PLH}	Propagation delay time, low-to-high level output (disable time)	from $\bar{E}$		30		ns
		from $\bar{W}$		35		
t_{EPD}	Chip power-down time		See Figure 1	65		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C

NOTE: 3. Load circuit and voltage waveforms are shown in Appendix A, page 44.

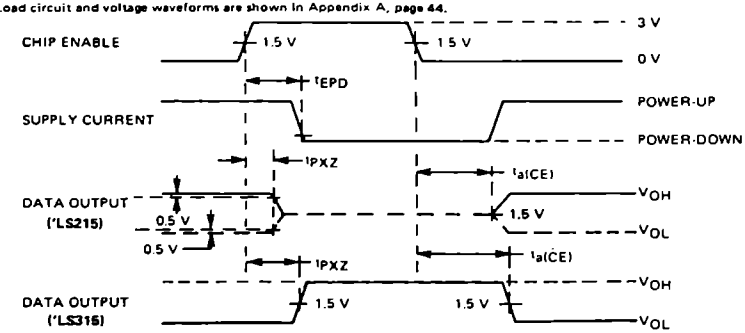


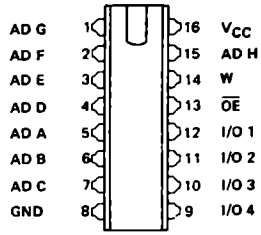
FIGURE 1. POWER-DOWN WAVEFORMS

1024-BIT EDGE-TRIGGERED RANDOM-ACCESS MEMORIES

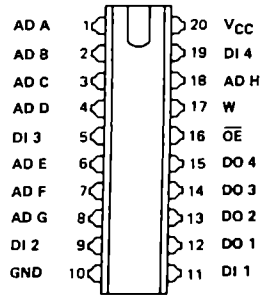
- Static Fully Decoded RAM's Organized as 256 Words of Four Bits Each
- Schottky-Clamped for High Performance
- Edge-Triggered Write Control
- 'S207 Data and Address are Same Pins as 1K PROM's (SN54S287, SN74S287, SN54S387, and SN74S387)
- High-Density Dual-in-Line Packages have Pin-Row Spacing of 0.300-Inch
- Three-State Output for Driving Bus-Organized Systems and/or Highly Capacitive Loads
- Compatible with Most TTL and I^2L Circuits
- Typical Performance:

TYPES	ACCESS TIMES		POWER
	WRITE	READ	DISS.
SN54S207/'S208	35 ns	40 ns	600 mW
SN54LS207/'S208	65 ns	75 ns	200 mW

SN54LS207,SN54S207 . . . J PACKAGE
SN74LS207,SN74S207 . . . J OR N PACKAGE
(TOP VIEW)



SN54LS208,SN54S208 . . . J PACKAGE
SN74LS208,SN74S208 . . . J OR N PACKAGE
(TOP VIEW)

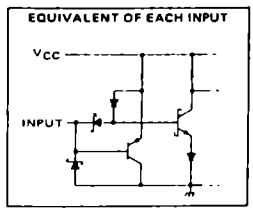


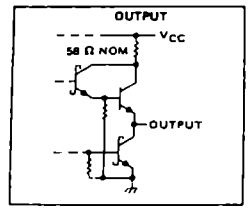
Pin assignments are same for all packages.

description

These 1024-bit active-element memories are monolithic transistor-transistor logic (TTL) arrays organized as 256 words of four bits each. They are fully decoded with output enable inputs to simplify decoding required to achieve the desired system organization. Read and write times are virtually equal, which simplifies control implementation.

schematics of inputs and outputs





write cycle

While the output-enable input, $\overline{OE}$, of the 'LS207, 'S207 is high, data applied to the input/output (I/O) is written into the selected location on a positive transition at the write input. Information at the data input of the 'LS208, 'S208 memory is written into the selected location on a positive transition at the write input regardless of the state of the output-enable input. While the output-enable input of either is high, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

read cycle

The stored information is available at the output when the output-enable input is low.

DESIGN GOAL
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

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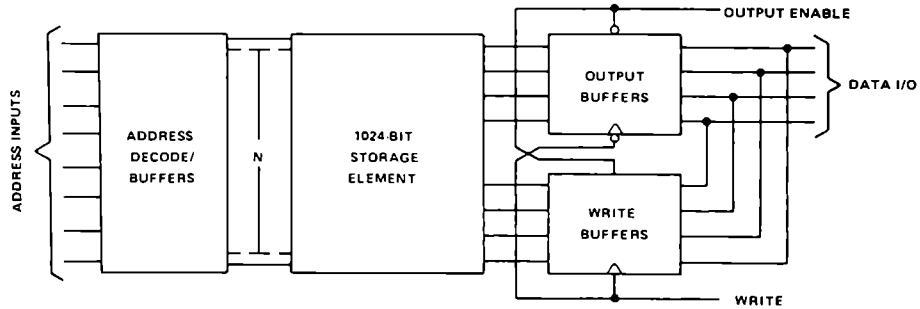
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,976.

'LS207, 'S207 functional block diagram

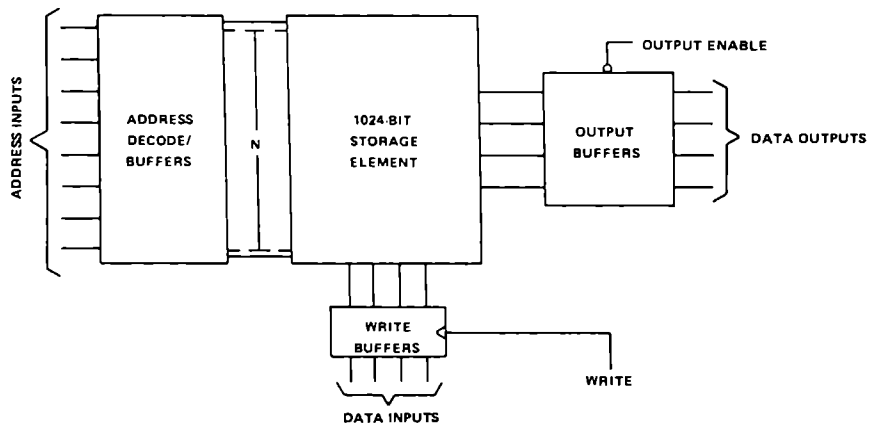


FUNCTION TABLE

FUNCTION	WRITE	ENABLE	OUTPUTS
WRITE	↑	H	Hi-Z (USE AS DATA INPUTS)
READ	H or L	L	DATA ADDRESSED
DO NOTHING	H or L	H	Hi-Z

H = HIGH, L = LOW, ↑ = LOW-TO-HIGH TRANSITION

'LS208, 'S208 functional block diagram



FUNCTION TABLE

FUNCTION	WRITE	ENABLE	OUTPUTS
WRITE AND READ	↑	L	DATA ADDRESSED
READ	H or L	L	DATA ADDRESSED
DO NOTHING	H or L	H	Hi-Z
WRITE ONLY	↑	H	HI-Z

H = HIGH, L = LOW, ↑ = LOW-TO-HIGH TRANSITION

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS', SN54S . . . . . −55°C to 125°C
SN74LS', SN74S . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

'S207, 'S208 recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−2			−6.5	mA
Low-level output current, I_{OL}				16			16	mA
Width of write pulse (high), $t_{w(wr)}$			15↑			15↑		ns
Setup time (see Figures 3 and 4)	Address before write, $t_{su(ad)}$		0↑			0↑		ns
	Data before write, $t_{su(da)}$		0↑			0↑		
Hold time	Output enable after write, $t_{h(\overline{OE})}$ (see Figure 3) 'S207	$t_{h(da)}$'			$t_{h(da)}$'			ns
	Address after write, $t_{h(ad)}$ (see Figures 3 and 4)		35↑			35↑		
	Data after write, $t_{h(da)}$ (see Figures 3 and 4)		35↑			35↑		
Operating free-air temperature, T_A (see Note 3)		−55		125	0		70	°C

↑ The arrow indicates that the rising transition of the write input is used for reference

'S207,'S208 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S'			SN74S'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input Clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	Off-state output current high-level voltage applied	'S207	V_{CC} = MAX,	V_{IH} = 2 V,			100			100	μA
		'S208	V_O = 2.4 V				50			50	
I_{OZL}	Off-state output current low-level voltage applied	'S207	V_{CC} = MAX,	V_{IH} = 2 V,			−250			−250	μA
		'S208	V_O = 0.5 V				−50			−50	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	'S207	V_{CC} = MAX,	V_I = 2.4 V			100			100	μA
		'S208					25			25	
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	'S207	V_{CC} = MAX,	See Note 2		120			120		mA
		'S208				120			120		

'LS207, 'LS208 recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−2			−6.5	mA
Low-level output current, I_{OL}				12			16	mA
Width of write pulse (high), $t_{w(wr)}$			25↑			25↑		ns
Setup time (see Figures 3 and 4)	Address before write, $t_{su(ad)}$		0↑			0↑		ns
	Data before write, $t_{su(da)}$		0↑			0↑		
Hold time	Output enable after write, $t_{h(\overline{OE})}$ (see Figure 3) 'S207	$t_{h(da)}$↑			$t_{h(da)}$↑			ns
	Address after write, $t_{h(ad)}$ (see Figures 3 and 4)		65↑			65↑		
	Data after write, $t_{h(da)}$ (see Figures 3 and 4)		65↑			65↑		
Operating free-air temperature, T_A (see Note 3)		−55		125	0		70	°C

↑The arrow indicates that the rising transition of the write input is used for reference.

'LS207, 'LS208 electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input Clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	Off-state output current high-level voltage applied	'LS207	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			100			100	μA
		'LS208					50			50	
I_{OZL}	Off-state output current low-level voltage applied	'LS207	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−250			−250	μA
		'LS208					−50			−50	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	'LS207	V_{CC} = MAX,	V_I = 2.4 V			100			100	μA
		'LS208					25			25	
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	'LS207	V_{CC} = MAX,	See Note 2		40			40		mA
		'LS208				40			40		

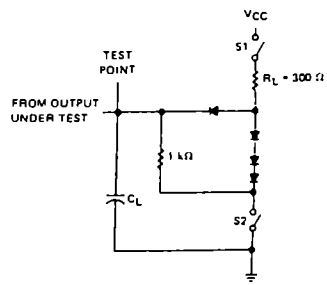
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25° C.
§Duration of the short-circuit should not exceed one second.
NOTES: 1. All voltage values are with respect to network ground terminal.
2. I_{CC} is measured with the write input high, output enable input grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	'S207, 'S208		'LS207,'LS208		UNIT
				TYP	MAX	TYP	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_L = 300 Ω, See Figures 1 thru 5	40		75		ns
$t_{a(\overline{OE})}$	Access time from output enable (enable time)			15		20		ns
$t_{a(wr)}$	Access time from write	'L5208, 'S208		25		50		ns
t_{PXZ}	Disable time from high or low level (see Note 4)	from OE§	C_L = 5 pF, R_{L1} = 300 Ω, See Figures 3 and 5	15		20		ns
		from W		15		20		

§This parameter defines the delay for the I/O port to enter the input mode.

PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance
All diodes are 1N3064

FIGURE 1 – LOAD CIRCUIT

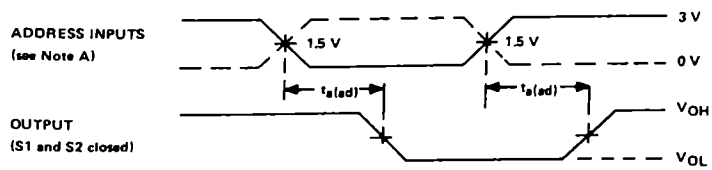


FIGURE 2 – ACCESS TIME FROM ADDRESS INPUTS
VOLTAGE WAVEFORMS

NOTE A. When measuring delay times from address inputs, the output-enable and write inputs are low.

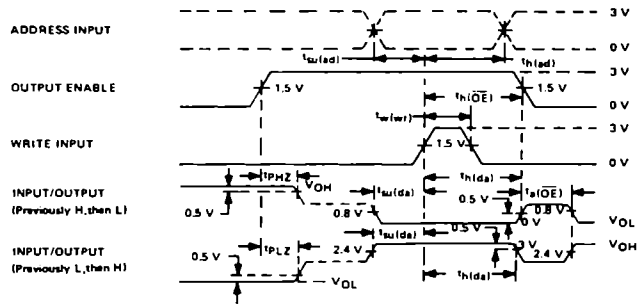


FIGURE 3 – 'LS207, 'S207 WRITE AND READ VOLTAGE WAVEFORMS

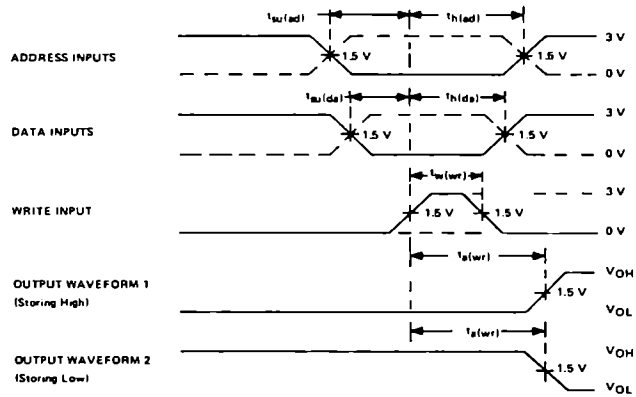


FIGURE 4 – 'LS208, 'S208 WRITE WHILE READ VOLTAGE WAVEFORMS (OUTPUT ENABLE IS LOW)

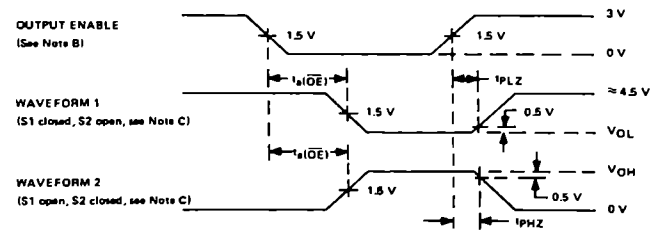


FIGURE 5 – ACCESS (ENABLE) TIME AND DISABLE TIME FROM OUTPUT ENABLE VOLTAGE WAVEFORMS

NOTES: B. When measuring delay times from the output-enable input, the address inputs are steady-state and the write/read input is low.
C. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
D. Input waveforms are supplied by the pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

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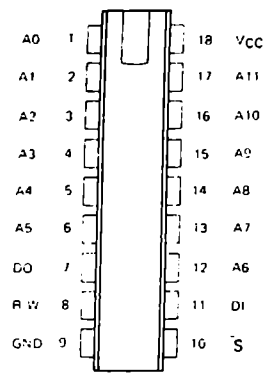
SN54S400, SN74S400, SN54S401, SN74S401
4096-BIT STATIC RANDOM-ACCESS MEMORIES

JULY 1978

- Organized as 4096 Words of 1 Bit Each
- Fully Static Storage
- High-Density 18-Pin Package
- Synchronous Operation with Latched Output Data
- Symmetrical Read/Write Performance
- Single 5-Volt Supply
- Fully TTL Compatible
- Choice of Three State (S400) or Open Collector (S401) Output
- Efficient High Performance Operation:
  - 75 ns Read Cycle
  - 75 ns Write Cycle
  - 500 mW Power Dissipation
  - (Typicals at 25°C)

18-PIN CERAMIC AND PLASTIC DUAL IN-LINE PACKAGES (TOP VIEW)



description

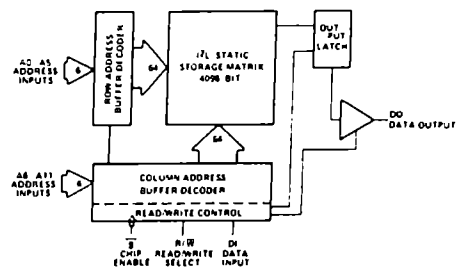
The 'S400 and 'S401 are monolithic, active-element, random-access memories with non-destructive data readout organized as 4096 words of 1 bit each. These RAMs integrate an I^2L static storage matrix with an edge-triggered Schottky-clamped forward transistor periphery to produce efficient, high performance operation.

Primary memory control is simplified to two pins: the R/$\overline{W}$ input which selects either the read or write mode of operation and the $\overline{S}$ input which serves the combined function of enabling or disabling the memory as well as triggering either the read or write cycle. Memory operation is therefore synchronous as a negative transition (↓) at $\overline{S}$ initiates execution of either the read or write cycle dependent on the state of the R/$\overline{W}$ input.

The 'S400 and 'S401 utilize separate pins for DI (data input) and DO (data output) with the DO buffer having a significantly faster disable than enable time. These features facilitate memory designs using either a separate or common I/O bus structure.

The 'S400, with a 3-state output, and the 'S401, with an open-collector output, are offered in both commercial 0 to 70°C (74S) and military −55 to 125°C (54S) temperature range versions.

functional block diagram



DESIGN GOALS
This document contains the design specifications for a product under development. Texas Instruments reserves the right to change these specifications in any manner, without notice.

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Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

FUNCTION TABLE

FUNCTION	$\overline{S}$ INPUT	R/$\overline{W}$ INPUT	OUTPUT
Read	↓	H	Active – Addressed Data
Hold	L	H	Active – Last Data
Inhibit	↑ or H	H	Hi-Z (OFF)
Write	↓	L	Hi-Z (OFF)
Inhibit	L or ↑ or H	L	Hi-Z (OFF)

H = high level, L = low level, ↑ = low-to-high transition, ↓ = high-to-low transition

read cycle

The read function is selected by applying a high logic level to the R/$\overline{W}$ input. If data is to be read from a newly addressed location, the R/$\overline{W}$ and A0-A11 inputs must be setup (t_{su}) prior to negative transition (↓) at the $\overline{S}$ input and be held (t_h) stable until completion of the read cycle. A negative transition at $\overline{S}$ strobes the periphery circuitry causing the addressed location to be sensed, latched and the output to become active presenting true data. Following a read cycle the output will remain active presenting true data until either the $\overline{S}$ input is taken high or the R/$\overline{W}$ input is taken low.

write cycle

The write function is selected by applying a low logic level to the R/$\overline{W}$ input. The DI, R/$\overline{W}$ and A0-A11 inputs must be setup (t_{su}) prior to a negative transition at $\overline{S}$ and be held (t_h) stable until completion of the write cycle. A negative transition at $\overline{S}$ will strobe the periphery circuitry causing DI to be stored in the addressed location and loaded into the output latch. Any time the R/$\overline{W}$ input is low, the device output will be at a high-impedance (off). This feature permits common I/O connection for bi-directional data bus designs.

ORDERING INFORMATION

PART NUMBER	AMBIENT TEMPERATURE RANGE	OUTPUT	PACKAGE (18 PIN)
SN74S400N	Commercial – 0 to 70°C	3-State	Plastic DIP
SN74S400J	Commercial – 0 to 70°C	3-State	Ceramic DIP
SN54S400J	Military – −55 to 125°C	3-State	Ceramic DIP
SN74S401N	Commercial – 0 to 70°C	Open-Collector	Plastic DIP
SN74S401J	Commercial – 0 to 70°C	Open-Collector	Ceramic DIP
SN54S401J	Military – −55 to 125°C	Open-Collector	Ceramic DIP

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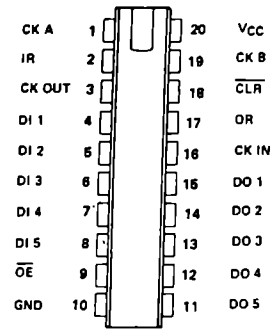
TYPE SN74S225
16 x 5 ASYNCHRONOUS FIRST-IN/FIRST-OUT MEMORY

SEPTEMBER 1976

- Independent Synchronous Inputs and Outputs
- Organized as 16-Words of 5 Bits
- DC to 10 MHz Data Rate
- 3-State Data Outputs
- 20-Pin, 300-mil, High Density Package

SN74S225 . . . J OR N PACKAGE
(TOP VIEW)



Pin assignments are same for all packages

description

This 80-bit active-element memory is a monolithic, Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words of five-bits each. The 'S225 can easily be expanded to 16N-words of 5N-bits in length and features a single enable control for all 3-state data outputs.

operation

A FIFO is a memory storage device which allows data to be written into and/or read from its array at independent data rates. The 'S225 is a FIFO which will process data at any desired clock rate from DC to 10 MHz. The data is processed in a parallel format, word by word.

Reading or writing is done independently utilizing separate synchronous data clocks. Data may be written into the array on the low-to-high transition of either load clock input. Data may be read out of the array on the low-to-high transition of the unload clock input (normally high). When writing data into the FIFO one of the load clock inputs must be held high while the other strobes in the data. This arrangement allows either load clock to function as an inhibit for the other.

Status of the 'S225 is provided by three outputs. Input ready monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload clock output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, output ready, is high when the first word location contains valid data and unload clock input is high. When unload clock input is low, output ready will be low. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are three-state with a common control input, output enable. When output enable is low, the data outputs are enabled to function as totem-pole outputs. A high-logic-level forces each data output to a high-impedance state while all other inputs and outputs remain active.

The clear input invalidates all data stored in the memory array by clearing the control logic and setting output ready to a low-logic-level on the high-to-low transition of a low-active pulse. The data outputs do not change as a result of the clear input; however, the output ready at a low-logic-level signifies invalid data.

TENTATIVE DATA SHEET
his document provides tentative information
n a new product. Texas Instruments reserves
ie right to change specifications for this
oduct in any manner without notice.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U. S. Patent Number 3,463,975.

FUNCTION TABLES

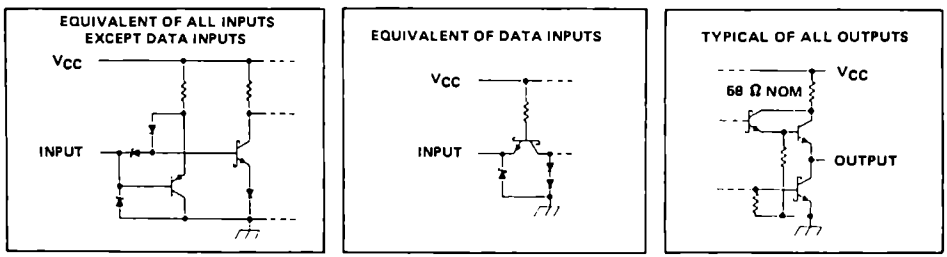
Table 1 – Input Functions

Input	Pin	Description
CK A	1	Load Clock A
DI 1 - DI 5	4-8	Data Inputs
$\overline{OE}$	9	Output Enable
CK IN	16	Unload Clock Input
$\overline{CLR}$	18	Clear
CK B	19	Load Clock B
GND	10	Ground pin
V_{CC}	20	Supply Voltage

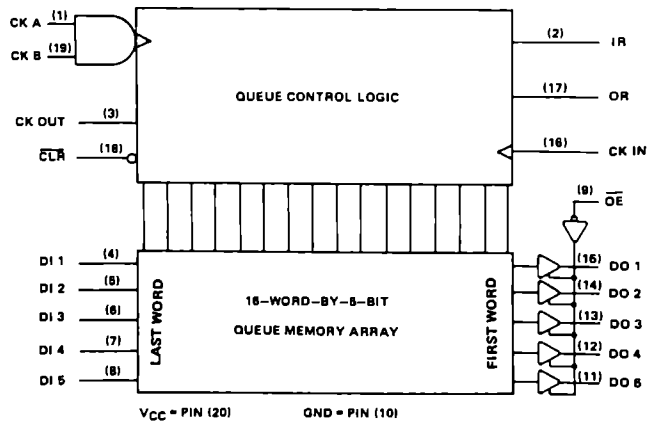
Table 2 – Output Functions

Output	Pin	Description
IR	2	Input Ready
CK OUT	3	Unload Clock Output
DO 5 - DO 1	11 - 15	Data Outputs
OR	17	Output Ready

schematics of inputs and outputs



functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (see Note 1) 7V
Input Voltage 5.5V
Off-State Output Voltage 5.5V
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	All Outputs Except Data			−3.2	mA
	Data Outputs			−6.5	
Low-level output current, I_{OL}	All Outputs Except Data			8	mA
	Data Outputs			16	
Pulse Width	Load Clock A or B, t_w (high)	25			ns
	Unload Clock Input, t_w (low)	7			
	Clear, t_w (low)	40			
Setup Time	Data to Load Clock, t_{su} (DI) See Note 2	−15↑			ns
	Clear Release to Load Clock, t_{su}	25↑			
Hold Time, Data from Load Clock, t_h(DI)		70↑			ns
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Data must be setup within 15 ns after the load clock positive transition.

↑ The arrow indicates that the low-to-high transition of the load clock is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	2.9		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX		0.35	0.50	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_O = 2.4 V			50	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_O = 0.5 V			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Data In	V_{CC} = MAX,	V_I = 2.7 V			40	μA
		All Inputs Except Data In					25	
I_{IL}	Low-level input current	Data In	V_{CC} = MAX,	V_I = 0.5 V			−1	mA
		All Inputs Except Data In					−250	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−30		−100	mA
I_{CC}	Supply Current		V_{CC} = MAX,	See Note 3		80	120	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Duration of the short circuit should not exceed one second.
NOTE 3: I_{CC} is measured with all inputs grounded and the output open.

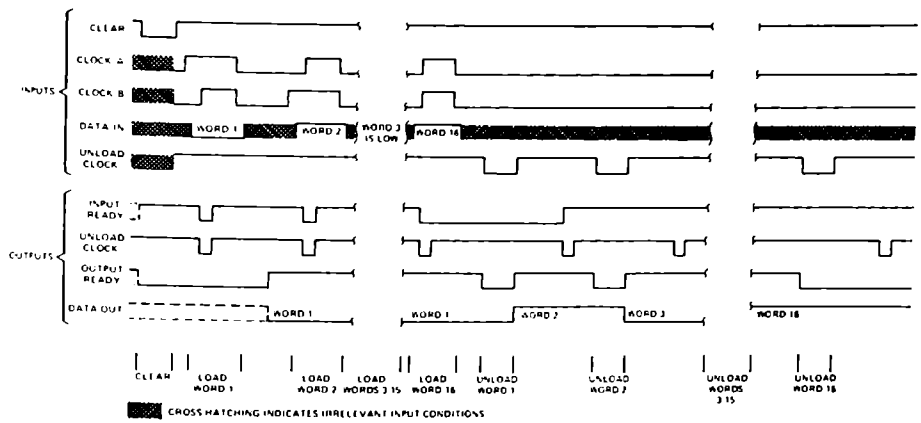
switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETERS¶	FROM	TO	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
f_{max}	CK A		C_L = 30 pF, R_L = 300 Ω, See Note 4	10	20		MHz
f_{max}	CK B			10	20		MHz
f_{max}	CK IN			10	20		MHz
t_w	CK OUT			7	14		ns
t_{PLZ}	$\overline{OE}$	DOi	C_L = 5 pF, R_{L1} = 300 Ω, See Note 4			40	ns
t_{PHZ}						40	
t_{PLH}	CK IN	DOi			50	75	ns
t_{PHL}					50	75	
t_{PLH}	CK A or CK B	OR			215	325	ns
t_{PLH}	CK IN	OR			40	60	ns
t_{PHL}					30	45	
t_{PHL}	$\overline{CLR}$	OR			40	60	ns
t_{PHL}	CK A or CK B	CK OUT	C_L = 30 pF, R_L = 300 Ω, See Note 4		35	50	ns
t_{PHL}	CK IN	CK OUT			300	450	ns
t_{PHL}	CK A or CK B	IR			42	65	ns
t_{PLH}	CK IN	IR			290	450	ns
t_{PLH}	$\overline{CLR}$	IR			20	35	ns
t_{PHL}							
t_{PLH}	OR↑	DOi			5	16	ns
t_{PHL}	OR↓				5	15	

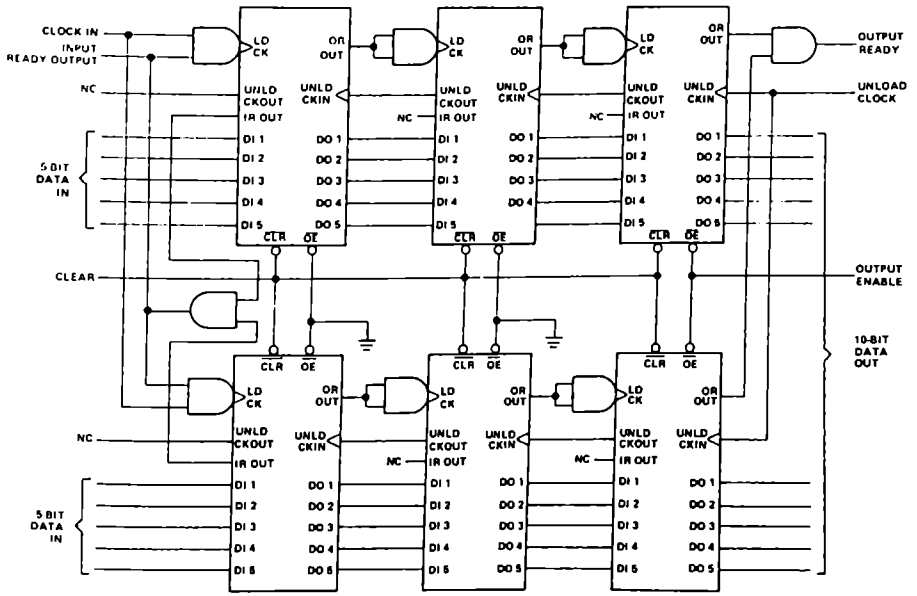
¶ f_{max} = maximum clock frequency.
t_w = pulse width (output)
↑↓ = The arrow indicates that the low-to-high (↑) or high-to-low (↓) transition of the output ready (OR) output is used for reference.
t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low-level output
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 4: Load circuit and voltage waveforms are shown in Appendix A.

TYPICAL WAVEFORMS

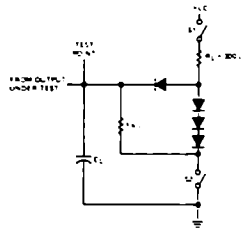


EXPANDING THE S225 FIFO
(48 WORDS OF 10 BITS SHOWN)



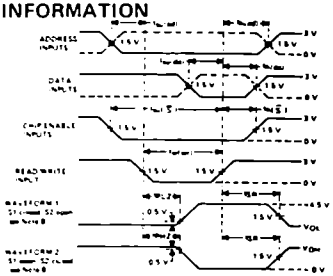
APPENDIX A

PARAMETER MEASUREMENT INFORMATION

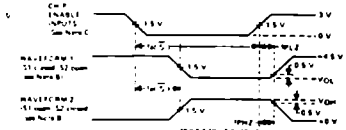


LOAD CIRCUIT

ACCESS TIME FROM ADDRESS INPUTS
VOLTAGE WAVEFORMS



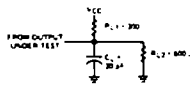
WRITE CYCLE VOLTAGE WAVEFORMS



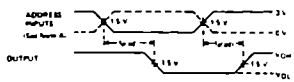
ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP ENABLE
VOLTAGE WAVEFORMS

NOTES. A. When measuring access times from address inputs, the enable/select input (s) is (are) low and the read/write input is high.
B. Waveform shown is for the output with internal conditions such that the output is low except when disabled.
C. When measureing access and disable times from enable/select input (s), the address inputs are steady-state and the read/write input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics and $Z_{out} \approx 50\ \Omega$

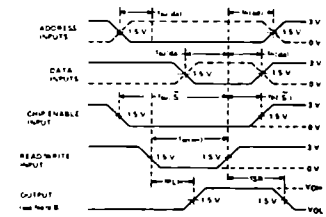
TESTING RAM's WITH 3-STATE OUTPUTS



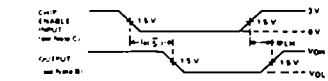
LOAD CIRCUIT



ACCESS TIME FROM ADDRESS INPUTS
VOLTAGE WAVEFORMS



WRITE CYCLE VOLTAGE WAVEFORMS



ACCESS (ENABLE) TIME AND DISABLE TIME FROM CHIP ENABLE
VOLTAGE WAVEFORMS

NOTES: A. When measuring access times from address inputs, the enable/select input (s) is (are) low and the read/write input is high.
B. Waveform shown is for the output with internal conditions such that the output is low except when disabled.
C. When measureing access and disable times from enable/select input (s), the address inputs are steady-state and the read/write input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics

TESTING RAM's WITH OPEN-COLLECTOR OUTPUTS

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The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

Bipolar Microcomputer Support Functions Data Manual

DECEMBER 1976

TEXAS INSTRUMENTS
INCORPORATED

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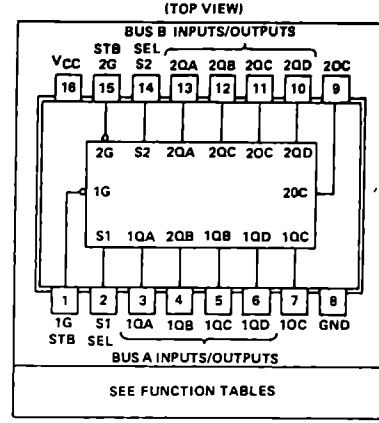
SN54S226, SN74S226
4-BIT PARALLEL LATCHED BUS TRANSCEIVERS

- Universal Transceivers for Implementing System Bus Controllers
- Dual-Rank 4-Bit Transparent Latches Provide
  - Exchange Data Between 2 Buses In One Clock Pulse
  - Bus-to-Bus Isolation
  - Rapid Data Transfer
  - Full Storage Capability
- Hysteresis at Data Inputs Enhances Noise Rejection
- Separate Output Control Inputs Provide Independent Enable/Disable for Either Bus Output
- 3-State Outputs Drive Bus Lines Directly

SN54S226.....J PACKAGE
SN74S226.....J OR N PACKAGE
(TOP VIEW)


BUS B INPUTS/OUTPUTS
STB SEL
VCC 2G S2 2QA 2QB 2QC 2QD 2QC
16 15 14 13 12 11 10 9
2G S2 2QA 2QC 2QC 2QD
1G
2QC
S1 1QA 2QB 1QB 1QD 1QC
1 2 3 4 5 6 7 8
1G S1 1QA 1QB 1QC 1QD 1QC GND
STB SEL
BUS A INPUTS/OUTPUTS
SEE FUNCTION TABLES

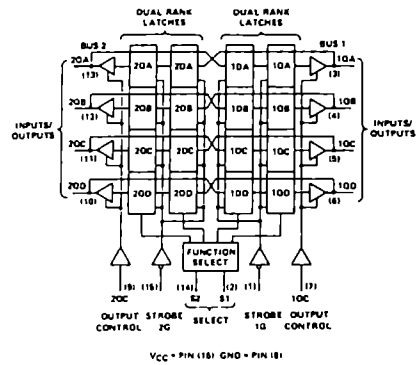
description

These high-performance Schottky TTL quadruple bus transceivers employ dual-rank bidirectional 4-bit transparent latches and feature 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The bus-management functions implemented and the high-impedance controls offered provide the designer with a controller/transceiver that interfaces and drives system bus-organized lines directly. They are particularly attractive for implementing:

Bidirectional bus transceivers
Data-bus controllers

The bus-management functions, under control of the function-select (S1, S2) inputs, provide complete data integrity for each of the four modes described in the function table. Directional transparency provides for routing data from-or-to either bus, and the dual store and dual readout capabilities can be used to perform the exchange of data between the two bus lines in the equivalent of a single clock pulse. Entry of data is accomplished by selecting the latch function, setting up the data, and taking the appropriate strobe input low. As long as the strobe is held low, the operation remains stable for the selected function. Further control is offered through the availability of independent output controls which can be used to enable

functional block diagram



DESIGN GOAL

1276 This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

BUS-MANAGEMENT FUNCTION TABLE

OPERATION	S2	S1	LATCH FUNCTIONS
DRIVE BUS 2	L	L	Pass Bus 1 Data to Bus 2
DRIVE BUS 1	H	L	Pass Bus 2 Data to Bus 1
EXCHANGE	H	H	Store Bus 1 and Bus 2 Data
BUS 1 & 2	L	H	Readout Stored Data

OUTPUT-CONTROL FUNCTION TABLE

2OC	1OC	OUTPUT FUNCTION
L	X	Disable Bus 1 Outputs (Hi-Z)
H	X	Enable Bus 1 Outputs
X	L	Disable Bus 2 Outputs (Hi-Z)
X	H	Enable Bus 2 Outputs

or disable the outputs as shown in the output-control function table, regardless of the latch function in process. Store operations can be performed with the outputs disabled to a high-impedance (Hi-Z). In the Hi-Z state the inputs/outputs neither load nor drive the bus lines significantly. The pnp inputs feature typically 400 millivolts of hysteresis to enhance noise rejection.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54S226	−55°C to 125°C
	SN74S226	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

		SN54S226			SN74S226			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−6.5			−10.3	mA
Data setup time, t_{su}	Data	5↑			3↑			ns
	Select	5↓			3↓			
Data hold time, t_h	Data	5↑			3↑			ns
	Select	5↓			3↓			
Operating free-air temperature, T_A		−55		125	0		70	°C

†The arrow indicates the transition of the enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage					2			V
V_{IL}	Low-level input voltage							0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	SN54S226	V_{CC} = MIN,	V_{IH} = 2 V,	SN54S226	2.4	3.3		V
		SN74S226	V_{IL} = 0.8 V,	I_{OH} = MAX	SN74S226	2.4	2.9		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA				0.5	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,				100	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,				−100	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V				100	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V				−300	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−50		−180	mA
I_{CC}	Supply current		V_{CC} = MAX See Note 2				125		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTE 2. I_{CC} is measured with all inputs (and outputs) grounded.

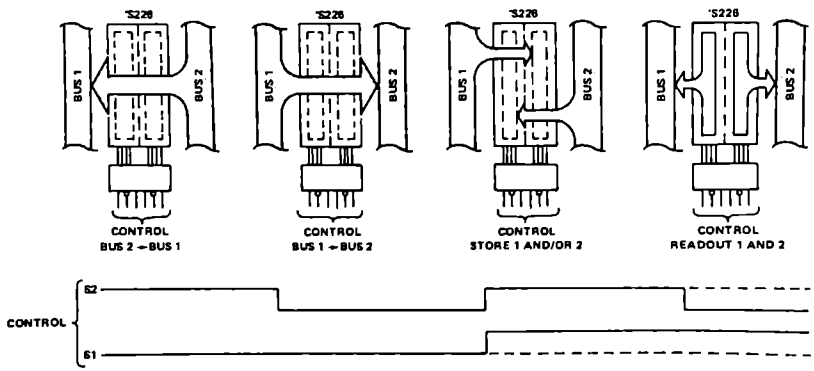
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Any Q	C_L = 50 pF, R_L = 280 Ω,		14		ns
t_{PHL}					14		
t_{PLH}	Select	Any Q			12		ns
t_{PHL}					12		
t_{PLH}	Strobe	Any Q			12		ns
t_{PHL}					12		
t_{ZH}	Output Control	Any Q			9		ns
t_{ZL}					9		
t_{HZ}	Output Control	Any Q	C_L = 5 pF, R_L = 280 Ω,		7		ns
t_{LZ}					7		

t_{PLH} = propagation delay time, low-to-high level
t_{PHL} = propagation delay time, high-to-low level
t_{ZH} = output enable time to high level
t_{ZL} = output enable time to low level
t_{HZ} = output disable time from high level
t_{LZ} = output disable time from low level

applications

The following examples demonstrate four fundamental bus-management functions which can be performed with the 'S226. Exchange of data on the two bus lines can be accomplished with a single high-to-low transition at S2 when S1 is high.



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TYPES SN54S240, SN54S241, SN74S240, SN74S241
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS
WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7812346, DECEMBER 1978

features:

- High-Performance Schottky TTL Line Drivers and/or Receivers in a High-Density 20-Pin Package
- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce D-C Loading on Bus Lines
- Hysteresis at Inputs Improve Noise Margins
- 'S241 Can Be Interconnected With No External Components to Perform as Bi-directional Bus Transceiver

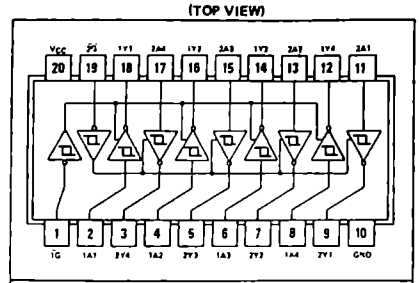
typical characteristics:

- Fan-Out:

	SN74S'	SN54S'
I_{OL} (Sink Current)	64 mA	48 mA
I_{OH} (Source Current)	−15 mA	−12 mA

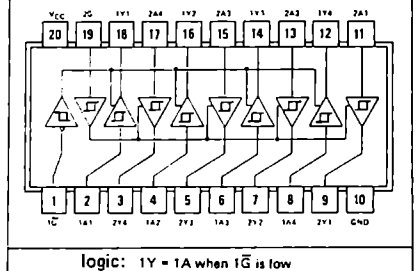
- Typical Propagation Delay Times:
  Data-to-Output:
  'S240 (Inverting) . . . 4.5 ns
  'S241 (Noninverting) . . . 6 ns
- Enable-to-Output . . . 9 ns

SN54S240 . . . J PACKAGE
SN74S240 . . . J OR N PACKAGE
(TOP VIEW)



logic: $1Y = 1\overline{A}$ when $1\overline{G}$ is low
$2Y = 2\overline{A}$ when $2\overline{G}$ is low
When $1\overline{G}$ is high 1Y outputs are at a high impedance
When $2\overline{G}$ is high 2Y outputs are at a high impedance

SN54S241 . . . J PACKAGE
SN74S241 . . . J OR N PACKAGE
(TOP VIEW)



logic: $1Y = 1A$ when $1\overline{G}$ is low
$2Y = 2A$ when $2G$ is high
When $1\overline{G}$ is high 1Y outputs are at a high impedance
When $2G$ is low 2Y outputs are at a high impedance

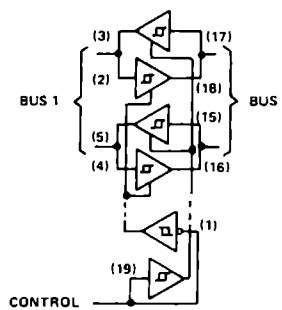
description

These buffers/line drivers are designed specifically to improve both the performance and p-c board density of 3-state buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 millivolts of hysteresis at each low-current p-n-p data-line input, they provide improved noise rejection and high-fan-out outputs to restore Schottky TTL levels completely, or the SN74S' versions can be used to drive terminated lines down to 133 Ω.

Typically, the 'S240 can replace the equivalent of six SN54S04, SN74S04 inverters or four SN54S130, SN74S140 line drivers at their rated drive capabilities with the added benefits of input hysteresis and 3-state outputs. The 'S241 offers the same complexity and drive capability but is designed for use in non-inverting applications.

In bus-organized systems, the 'S241 can be connected with no external components to perform as a non-inverting input/output bus transceiver. With complementing enable inputs, the control function can be connected directly to both enable inputs while the two 4-line data paths can be connected (at adjacent pins) input-to-output on both sides to form the asynchronous transceiver/buffer.

'S241 BUS TRANSCEIVER



L . . . RECEIVE BUS 1 DRIVE BUS 2
H . . . RECEIVE BUS 2 DRIVE BUS 1

TENTATIVE DATA SHEET
This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

recommended operating conditions

PARAMETER	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			48			64	mA
Operating free-air temperature, T_A (see Note 2)	−55		125	0		70	°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			'S240			'S241			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −3 mA	V_{IL} = 0.8 V,		2.4	3.4		2.4	3.4		V
			V_{CC} = MIN, I_{OH} = MAX	V_{IL} = 0.5 V,		2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN,	I_{OL} = MAX				0.55			0.55	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V				50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.5 V				−50			−50	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current, any input		V_{CC} = MAX,	V_{IH} = 2.7 V				50			50	μA
I_{IL}	Low-level input current	Any A	V_{CC} = MAX,	V_{IL} = 0.5 V				−400			−400	μA
		Any G						−2			−2	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−50		−225	−50		−225	mA
I_{CC}	Supply current	Total, outputs high	V_{CC} = MAX, Outputs open		SN54S'		80	123		95	147	mA
					SN74S'		80	135		95	160	
		Total, outputs low			SN54S'		100	145		120	170	
					SN74S'		100	150		120	180	
		Outputs at Hi-Z			SN54S'		100	145		120	170	
					SN74S'		100	150		120	180	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'S240			'S241			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Note 3	R_L = 90 Ω,		4.5	7		6	9	ns
t_{PHL}	Propagation delay time, high-to-low-level output				4.5	7		6	9	ns
t_{ZL}	Output enable time to low level				10	15		10	15	ns
t_{ZH}	Output enable time to high level				6.5	10		8	12	ns
t_{LZ}	Output disable time from low level	C_L = 5 pF,	R_L = 90 Ω		10	15		10	15	ns
t_{HZ}	Output disable time from high level				6	9		6	9	ns

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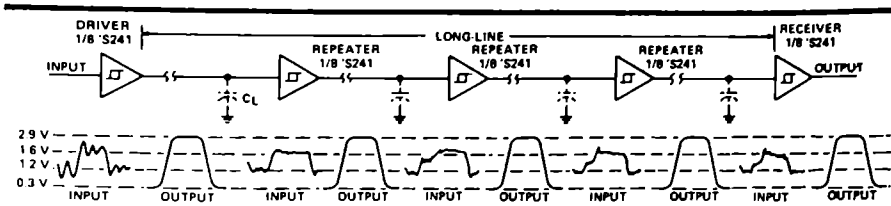
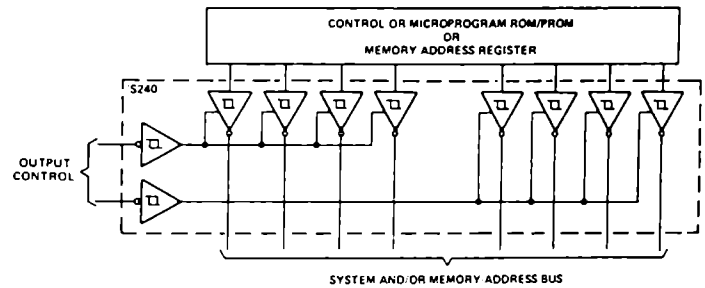
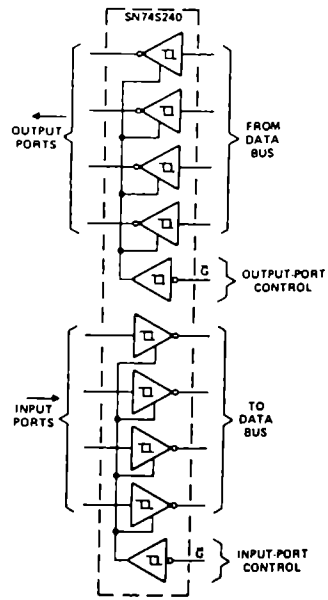


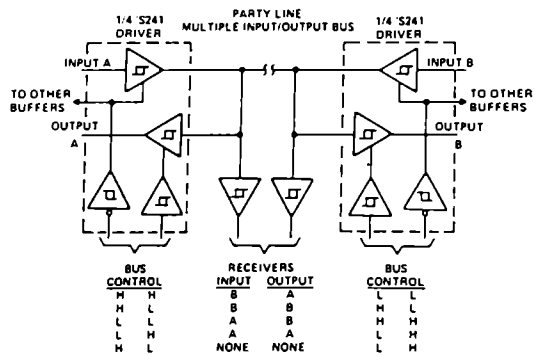
'S241's USED AS REPEATER/LEVEL RESTORER



'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS
IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM
WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

5

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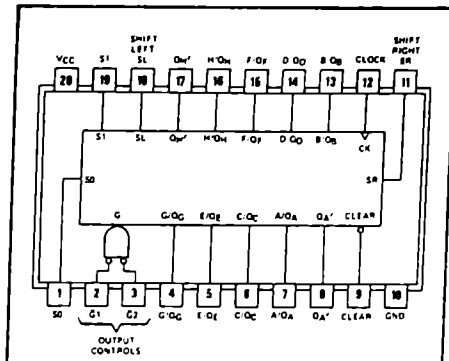
TYPES SN54S299, SN74S299
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

DECEMBER 1976

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
  Hold (Store) Shift Left
  Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can be cascaded for N-Bit Word Lengths
- Applications:
  Stacked or Push-Down Registers,
  Buffer Storage, and
  Accumulator Registers

SN54S299 . . . J PACKAGE
SN74S299 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description and function table

description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

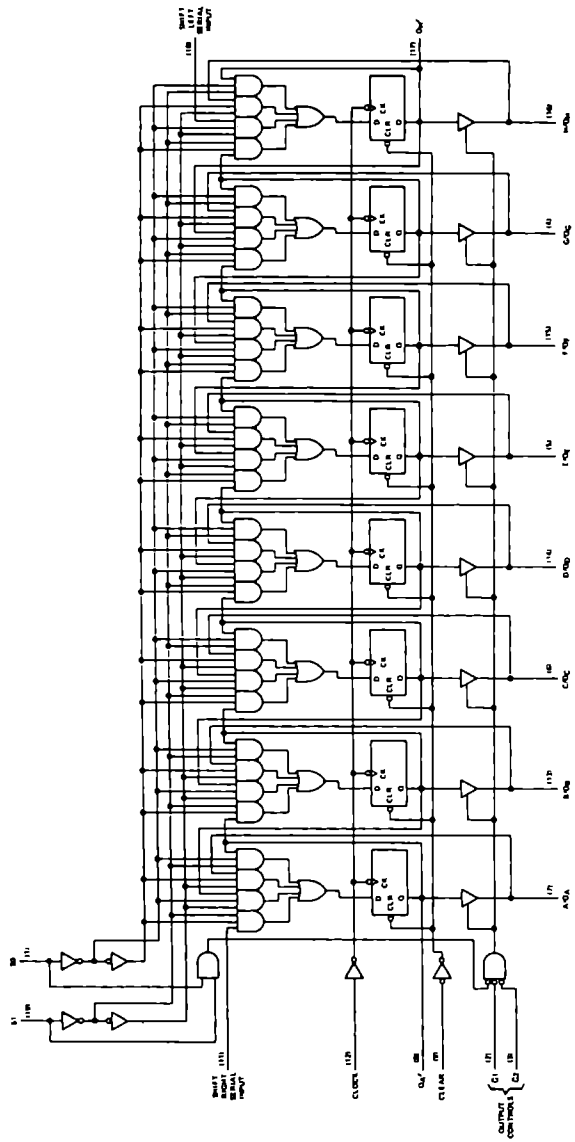
MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

functional block diagram



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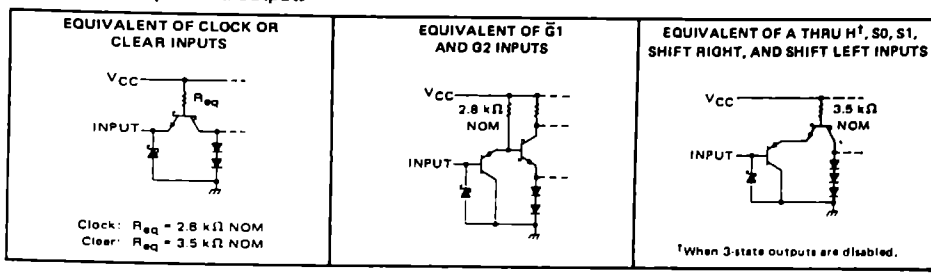
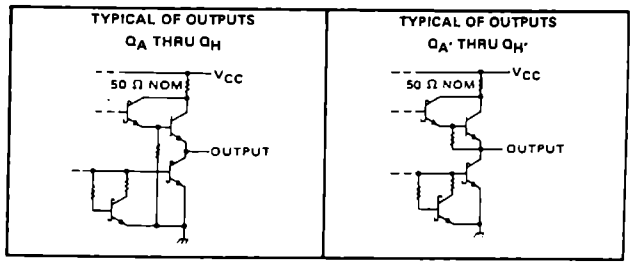
schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input Voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S299 (see Note 2) . . . . . −55°C to 125°C
SN74S299 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTES 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S299			SN74S299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			−2			−6.5	mA
	$Q_{A'}$ or $Q_{H'}$			−0.5			−0.5	
Low-level output current, I_{OL}	Q_A thru Q_H			20			20	mA
	$Q_{A'}$ or $Q_{H'}$			6			6	
Clock frequency, f_{clock}		0		50	0		50	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	10			10			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$	Clear low	10			10			ns
Setup time, t_{su}	Select	15†			15†			ns
	High-level data◇	7†			7†			
	Low-level data◇	5†			6†			
	Clear inactive-state	10†			10†			
Hold time, t_h	Select	5†			5†			ns
	Data◇	6†			5†			
Operating free-air temperature, T_A		−55		125	0		70	°C

◇Data includes the two serial inputs and the eight input/output data lines.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.2		V
		$Q_{A'}$ or $Q_{H'}$	V_{IL} = 0.8 V,	I_{OH} = MAX	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			100	μA
I_{OZL}	Off-state output current low-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−250	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	A thru H, S0, S1	V_{CC} = MAX,	V_I = 2.7 V			100	μA
		Any other					50	
I_{IL}	Low-level input current	Clock or clear	V_{CC} = MAX,	V_I = 0.5 V			−2	mA
		Any other					−250	μA
I_{OS}	Short-circuit output current§	Q_A thru A_H	V_{CC} = MAX		−40		−100	mA
		$Q_{A'}$ or $Q_{H'}$			−20		−100	
I_{CC}	Supply current		V_{CC} = MAX			140	225	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	50	70		MHz
t_{PLH}	Clock	$Q_{A'}$ or $Q_{H'}$	C_L = 15 pF, R_L = 1 KΩ, See Note 2		12	20	ns
t_{PHL}					13	20	
t_{PHL}	Clear	$Q_{A'}$ or $Q_{H'}$			14	21	ns
t_{PLH}	Clock	Q_A thru Q_H	C_L = 45 pF, R_L = 280 Ω, See Note 2		15	21	ns
t_{PHL}					15	21	
t_{PHL}	Clear	Q_A thru Q_H			16	24	ns
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			10	18	ns
t_{PZL}					12	18	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	C_L = 5 pF, R_L = 280 Ω, See Note 2		7	12	ns
t_{PLZ}					7	12	

¶ f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level
NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

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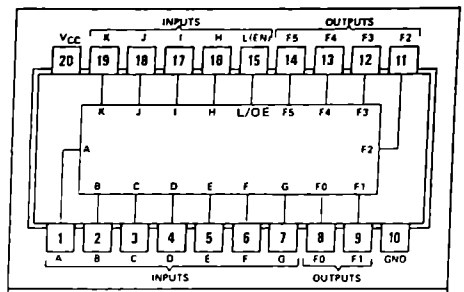
TYPES SN54S330, SN54S331, SN74S330, SN74S331
EXPANDABLE 12-INPUT, 50-TERM
FIELD-PROGRAMMABLE LOGIC ARRAYS

DECEMBER 1976

- Field-Programmable Logic Array Organized 12-Inputs/50-Product Terms/6-Outputs
- Programmable Options Include:
  - Active High or Low Inputs/Outputs
  - Choice of Dedicated Enable Input or Automatic Enable by True Product Terms
- Number of Inputs, Outputs, and Product Terms are Expandable
- High Density 20-Pin Package
- Full Schottky Clamping for High-Performance:
  - 35 ns Typical Data Delay Time
  - 20 ns Typical Enable Time
- Reliable TI-W Fuse Links for Fast, Low-Voltage Programming
- Choice of 3-State ('S330) or 2.5 kΩ Passive-Pullup ('S331) Outputs

SN54S330, SN54S331 . . . J PACKAGE
SN74S330, SN74S331 . . . J OR N PACKAGE


INPUTS
OUTPUTS
VCC
K J I H L(EN) F5 F4 F3 F2
20 19 18 17 16 15 14 13 12 11
K J I H L/OE F5 F4 F3
A
F2
B C D E F G F0 F1
1 2 3 4 5 6 7 8 9 10
A B C D E F G F0 F1 GND
INPUTS
OUTPUTS

positive logic: See description and function tables.

description

These high-performance, Schottky-clamped 12-input, 6-output logic arrays can be field programmed to provide 50 product terms derived from the 12 inputs and sum the 50 products onto 6-output lines. They feature a programmable option which permits the FPLA outputs to be automatically enabled by a true product term or, to dedicate during programming, input (L/OE) to serve as an output enable (OE). Either option makes the FPLA expandable with respect to product terms.

For every product term, 12 input variables can be programmed as high or low. Logic flexibility is further enhanced by the feature that the six outputs can be programmed individually to be active high or low.

The SN54S/74S330 is implemented with bus-driving 3-state outputs and can be connected directly to similar outputs in a bus-organized system. The SN54S/74S331 is implemented with a 2.5 kΩ passive pull-up resistor on each output meaning that:

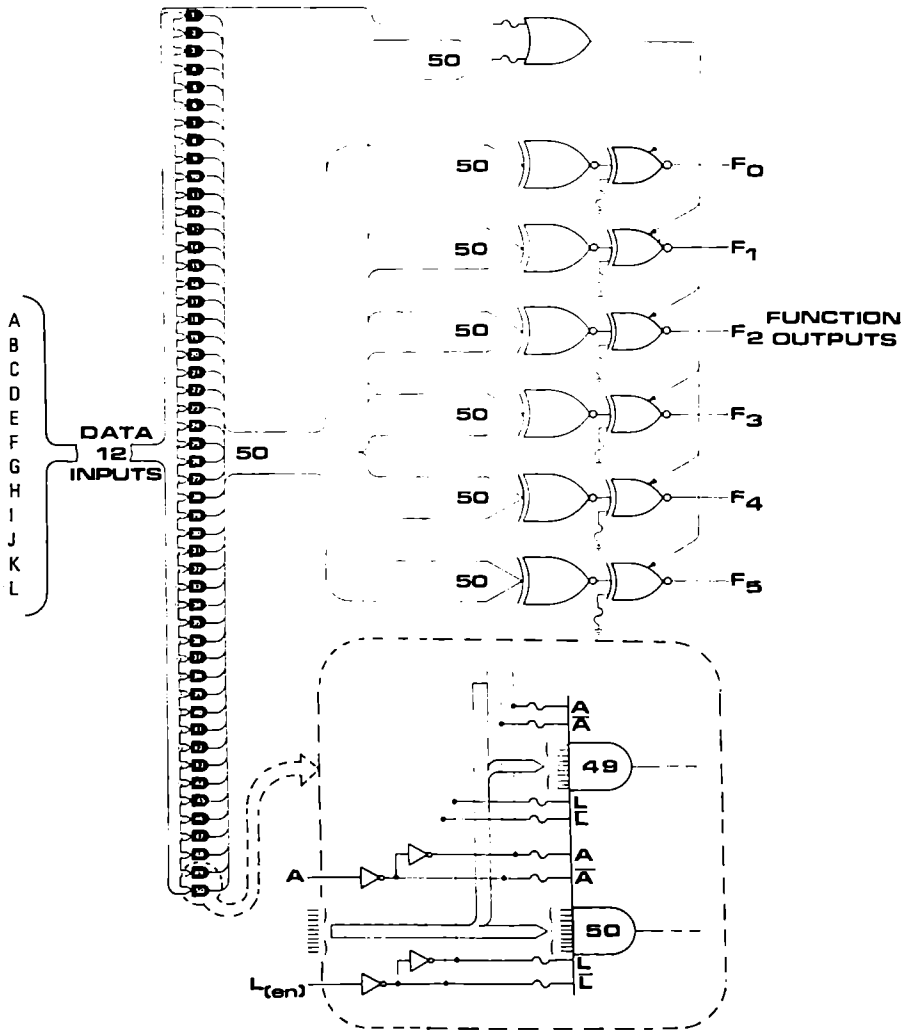
a. The output can be combined with other similar or open-collector outputs to perform the logical wire-AND or a simple enable/disable function.

b. The series SN74S' outputs are also rated to source 250 μA of current at V_{OH} = 3.7 minimum for direct interface with MOS input thresholds.

The TI-W fuse links, used in the 'S330/'S331, feature the same low-voltage programming characteristics and proven reliability which Texas Instruments PROM's have demonstrated over a number of years.

DESIGN GOAL
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.



WHERE:

$F_i = F_0, F_1, F_2, F_3, F_4,$ or F_5

$(ABC \ldots . L)_i$ = 12 PROGRAMMABLE INPUTS (H = TRUE OR L = TRUE) FOR EACH OF 50 PRODUCT TERMS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S330, SN54S331 . . . . . −55°C to 125°C
SN74S330, SN74S331 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S330, SN54S331			SN74S330, SN74S331			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	'S330 (T-S)			−2			−6.5	mA
	'S331 (2.5 kΩ Pullup)			−0.2			−0.25	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S330, SN54S331			SN74S330, SN74S331			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	'S330	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = MAX	2.4	3.4		2.4	3.1		V
		'S331		I_{OH} = MAX	3.7	4.5		3.7	4.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	'S330	V_{CC} = MAX	V_O = 2.4V			50			50	μA
I_{off}		'S331		V_O = 2.4V			50			50	
I_{OZL}	Off-state output current, low-level voltage applied	'S330	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}	Short-circuit output current§	'S330	V_{CC} = MAX		−30		−100	−30		−100	mA
		'S331			−1.4		−4.4	−1.4		−4.4	
I_{CC}	Supply current	'S330	V_{CC} = MAX,	See Note 2		110			110		mA
		'S331				122			122		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output of the 'S330 should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any input	Any output	C_L = 30 pF		35		ns
t_{PHL}					35		
t_{ZL}	Enable	Any output			15		ns
t_{ZH}					15		
t_{HZ}	Enable	Any output	C_L = 5 pF		15		ns
t_{LZ}					15		

programming the FPLA

The 'S330 and 'S331 are fabricated to include reliable low-voltage programmable Ti-W fuse links which have identical fusing characteristics with those used in TI's PROM's. The conditions recommended for programming the FPLA are virtually identical to those used for TI's PROM's; however, the AND-OR combinational logic performed by an FPLA requires that sequential programming be employed which establishes the AND term including the data/enable L/OE input before the OR term. Programming the automatic enable feature active, the true/false logic level of the outputs, and the data/enable input (L/OE) can be accomplished before or after the AND and OR matrices are established.

recommended conditions for programming

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)		4.75	5	5.75	V
Program pulse voltage, $V_{(pr)}$ (see Note 1)		10	10.5	11†	V
Program pulse rise time			100		ns
Input voltage (see Note 1)	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Voltage applied to output for OR programming, $V_{O(pr)}$ (see Figure D)		0	0.25	0.3	V
Duration of programming pulse Y (see Figures A, C, D, and Note 2)		0.9	1	20	ms
Programming duty cycle			25	35	%
Free-air temperature		0		55	°C

† Absolute maximum ratings.

NOTES: 1. Voltage values are with respect to the GND terminal.
2. Programming is guaranteed if the pulse applied is 0.9ms long. Typically, programming occurs in 1 ms.

programming the true/false logic level of the outputs

The FPLA is supplied with internal conditions established such that when a programmed AND or $\overline{\text{AND}}$ input term is true the associated function output (F_n) will be at a high logic level voltage, V_{OH}.

Programming the output to provide a low logic level voltage (V_{OL}) when the programmed input term is true can be accomplished by using AND/$\overline{\text{AND}}$ terms 50 through 55 shown in Table I and fusing the desired outputs using the step-by-step procedure.

TABLE I – ADDRESSES FOR PROGRAMMING OUTPUT LEVELS AND ENABLES

ADDRESS APPLIED TO OUTPUTS						PRODUCT TERM	PROGRAMS
F_5	F_4	F_3	F_2	F_1	F_0	ADDRESSED	
H	H	L	L	H	L	50	Output F_5 true low
H	H	L	L	H	H	51	Output F_4 true low
H	H	L	H	L	L	52	Output F_3 true low
H	H	L	H	L	H	53	Output F_2 true low
H	H	L	H	H	L	54	Output F_1 true low
H	H	L	H	H	H	55	Output F_0 true low
H	H	H	L	L	L	56	L/OE input into logical product term
H	H	H	L	L	H	57	Automatic output enable active

Programming can be verified before AND-OR programming by applying V_{CC} = 5 V and measuring $V_{OL} \leq 0.5$ V at the programmed output(s). After programming this test can be made by applying the input conditions which correspond to each term programmed to result in an active low-level output.

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step-by-step programming procedure for outputs and enables

1. Apply steady-state supply voltage (V_{CC} = 5 V) and disable the outputs by applying 10.5 volts to the 12 data inputs. See Figure 1.
2. Verify that the fuse link needs to be programmed. If not, proceed to the next term.
3. Only one fuse link is programmed at a time. Address the term to be programmed by applying V_{IH} and V_{IL} to the outputs in accordance with Table I.
4. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
5. After the Y pulse time (1 ms) is reached, V_{CC} should be stepped down to 5V at which level verification can be accomplished.
6. The data inputs may be taken to logic levels (to permit program verification) 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
7. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 6 for each function to be programmed.

NOTES 3: V_{CC} should be removed between program-pulses to reduce dissipation and chip temperatures. See Figure 1.

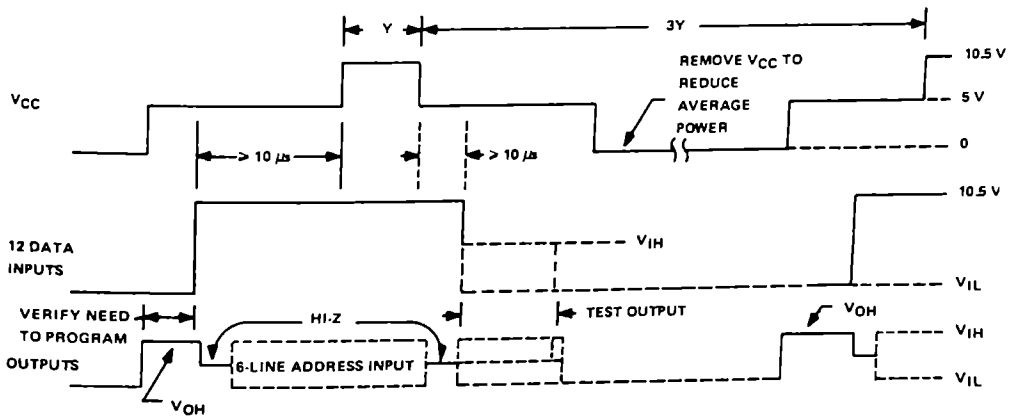

FIGURE 1 – OUTPUTS AND ENABLES PROGRAMMING SEQUENCE

programming the $L_{(en)}$ input

The L/OE input must be programmed either to function as a dedicated enable or to function as the 12th data input.

If it is to become the 12th data input a single fuse, at term 56_2 (see Table I), should be programmed in accordance with steps 1 through 4 above; then, input L is programmed logically into each AND/$\overline{\text{AND}}$ product term.

If input L/OE is to function as a dedicated output enable, term 66_2 is not fused: however, both AND/AND fuse links at each of the 50 product term addresses must be fused as outlined below creating a "don't care" for input L. This causes the input to become an overriding output enable/disable for the package.

programming the automatic disable to be inactive

The 'S330 and 'S331 are supplied with fuse links completing a circuit which automatically disables the six outputs (high-impedance (Z) for 'S330, high (H) for 'S331) for any product term which is purely "don't care"; i.e., not decoded by the AND matrix. Fusing one link inactivates the automatic output enabling circuit resulting in the six outputs being enabled for any input term, even "don't care".

The automatic disable fuse is programmed inactive by addressing term 57_2 (see Table I) and fusing in accordance with the step-by-step procedure above.

programming the AND/$\overline{\text{AND}}$ product terms

Each of the 50 product terms are capable of being programmed to decode a 12-wide term consisting of any combination of active (true) high, active (true) low, or don't care (H or L) input conditions at each of the 12 lines. This capability is implemented by providing AND/NAND decode input gates each having a pair of associated fusible links which can be programmed to inactivate the unused decode level. Both decode levels can be removed resulting in a "don't care" input. The equivalent logic diagram showing the fusible links is shown in Figure 2.

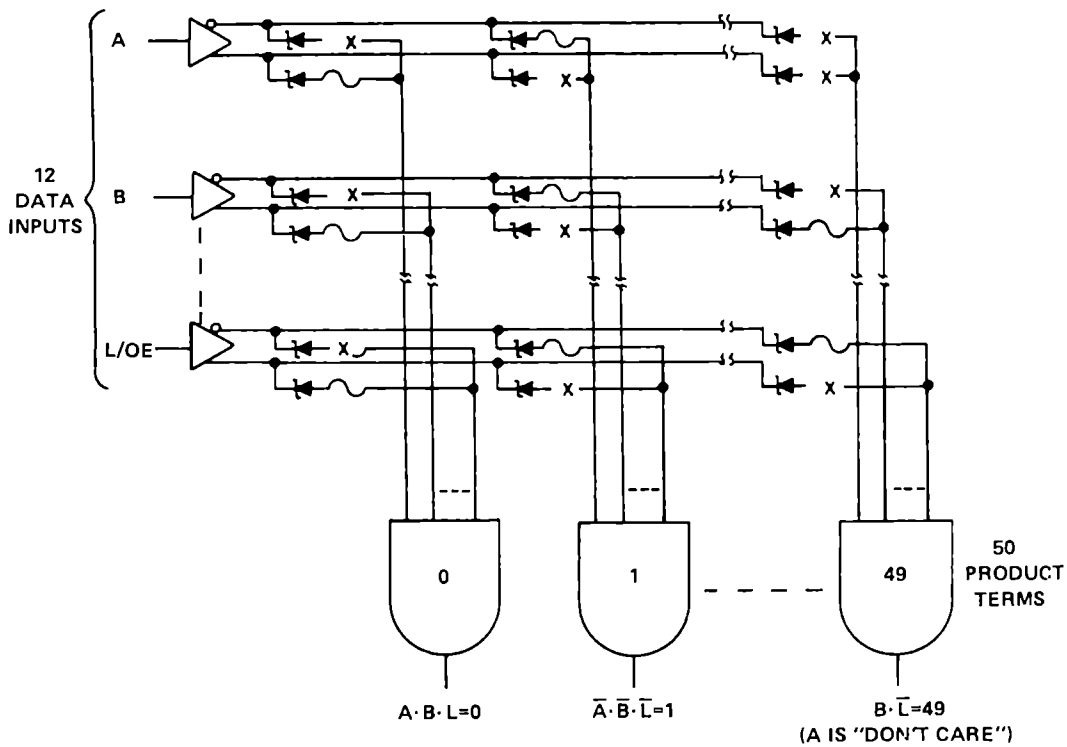

FIGURE 2 – EQUIVALENT LOGIC DIAGRAM OF FPLA PRODUCT TERMS

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A particular pattern is assumed to have been programmed into the AND/$\overline{\text{AND}}$ fuse matrix with fused links opened at the locations marked with an "X". The resultant product terms are enumerated for the outputs of each product-term AND gate.

Product terms programmed into the AND/AND matrix will be used to select the term for programming the OR (summing) matrix. Redundant product terms will select two sum terms in the OR matrix, and overlapping product terms may select two or more sum terms. Reliable programming can be accomplished if redundant product terms are avoided and overlapping product terms are made unique for programming.

Redundant product terms are defined as being absolutely equal; i.e., $A\bar{B}CD\bar{E}FG \equiv A\bar{B}CD\bar{E}\bar{F}G$. Use of apparently redundant terms is possible if the term does not use all inputs as the remaining inputs can be utilized to create unique terms for programming purposes by expansion:

Example:

$$A\bar{B}CD\bar{E}FGH \equiv A\bar{B}CE\bar{D}FG\bar{H}$$

After programming the OR matrix, the product terms can be readdressed and the H input can be programmed "don't care".

Overlapping terms are defined as two or more product terms in which the lesser product term can be addressed as a result of the application of a larger product term.

Examples:

$A\bar{B}CD\bar{E}FG$ ◄——— This large product term

$A\bar{B}\ D\bar{E}\ G$ ◄
$A\ CD\ F$ ◄ ——— also addresses these small terms

The small terms can be made unique for programming by simply expanding to non-redundant inputs.

$A\bar{B}CD\bar{E}FG$ ◄——— Large term

$A\bar{B}\ D\bar{E}\bar{F}G$ ◄
$A\ CD\ \bar{F}\bar{G}$ ◄ ——— Small terms made unique by expanding (one fuse link each)

After programming the OR matrix, the product terms can be shortened by readdressing each and programming the added inputs to a "don't care". The AND/$\overline{\text{AND}}$ matrix is programmed one fuse at a time by addressing the term in accordance with Table II and fusing the input while applying the logic level desired to be active. See Figure 3.

TABLE II – ADDRESSES FOR PROGRAMMING PRODUCT TERMS

ADDRESS APPLIED TO OUTPUTS						PRODUCT TERM
F_5	F_4	F_3	F_2	F_0	F_1	ADDRESSED
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
						.
						.
						.
H	H	L	L	L	L	48
H	H	L	L	L	H	49

step-by-step programming procedure for AND matrix

1. Apply steady-state supply (V_{CC} = 5 V) and disable the outputs by applying 10.5 volts to the 12 data inputs. See Figure 3.
2. Verify that the fuse link needs to be programmed. If not, proceed to the next term.
3. Only one fuse link is programmed at a time. Address the term to be programmed by applying V_{IH} and V_{IL} to the outputs in accordance with Table II.
4. Apply the level to be true at the input to be programmed.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. After the Y pulse time (1 ms) is reached, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
7. The data inputs may be taken to logic levels (to permit program verification) 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
8. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 7 for each input to be programmed.

NOTES: 4. V_{CC} should be removed between program pulses to reduce dissipation and chip temperatures. See Figure 3.
5. If the input just programmed is to be a "don't care" and is not being used to expand the product term repeat steps 4 and 5 with the opposite logic level applied to the input. Before changing the product term address, program all inputs (A through L/OE for this product term including all "don't cares".
6. If input L/OE is to be used as a dedicated package enable it must be programmed as a "don't care" by fusing both links at each of the 50 product term locations

The OR (summing) matrix for each product term can be programmed immediately upon completion of the 12-wide AND/$\overline{\text{AND}}$ term associated with it; or, the entire AND/$\overline{\text{AND}}$ term matrix can be programmed for all 50 product terms before programming the summing matrix.

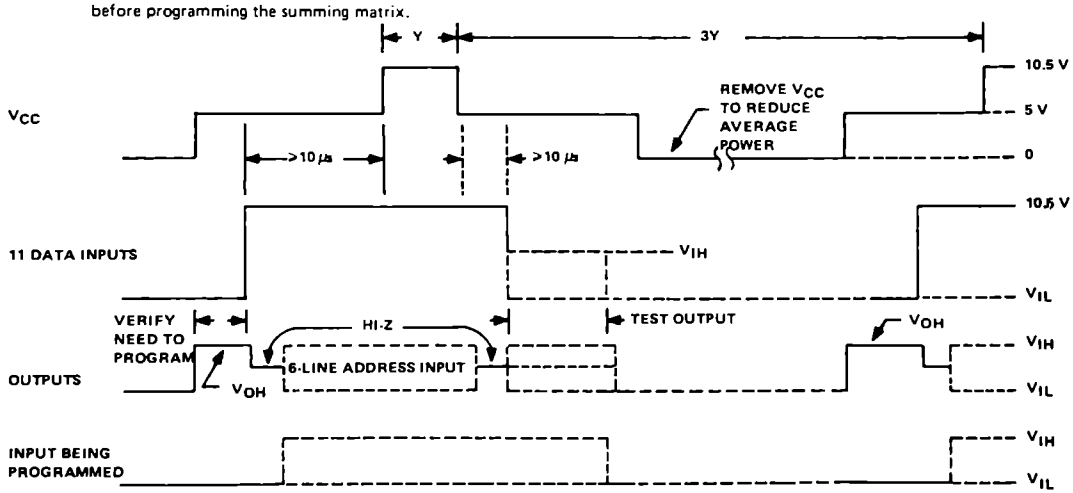

FIGURE 3 – AND MATRIX PRODUCT TERM PROGRAMMING SEQUENCE

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programming the OR (summing) matrix

Product term(s) programmed into the AND/$\overline{\text{AND}}$ matrix can now be selected to provide a true logic level output. The true logic level output at F_0 through F_5 will be high if the output polarity fuses are intact, or F_0 through F_5 will be low if the output polarity fuses have been programmed, or a combination of highs and lows if some of the output polarity fuses have been programmed.

step-by-step programming procedure for OR matrix

Programming the OR matrix consists of fusing (one at a time) those outputs (F_0 through F_5) which are desired to be false in the addressed product term. The procedure is:

1. Apply steady-state supply voltage (V_{CC} = 5 V) and apply the unique product term. See Figure 4.
2. Verify that the fuse link needs to be programmed. If not, proceed to the next fuse link.
3. Only one fuse link is programmed at a time. Enable the term to be programmed by applying $V_{O(pr)}$ to the first output to be false in the product term.
4. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
5. After the Y pulse time (1 ms) is reached, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
6. Program verification can occur 10 μs or more after V_{CC} reaches its steady-state value of 5 V.
7. At a Y pulse duty cycle of 35% or less repeat steps 1 through 6 for each output to be programmed false for the active product term.

NOTES. 7. V_{CC} should be removed between program pulses to reduce dissipation and chip temperatures. See Figure 1.
8. If product terms were expanded to make them unique for programming purposes the product terms can be addressed and the added inputs can be removed by programming them to a "don't care" (fuse the remaining links).

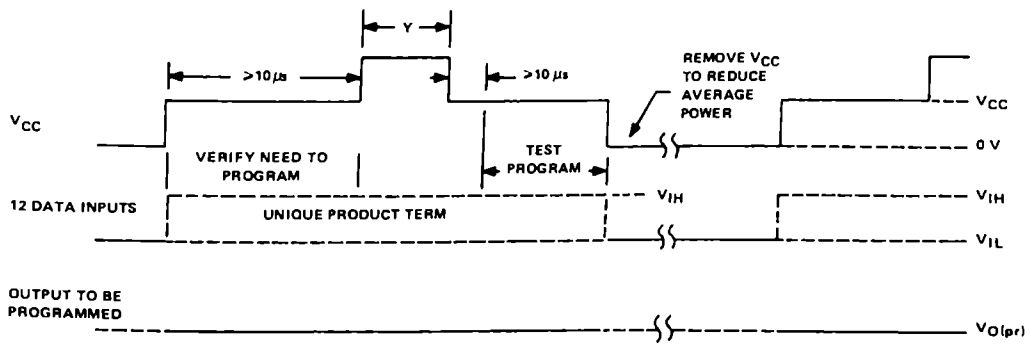

FIGURE 4 – OR TERM PROGRAMMING SEQUENCE

TYPES SN54S330, SN54S331, SN74S330, SN74S331
12-INPUT/6-OUTPUT EXPANDABLE FIELD-PROGRAMMABLE LOGIC ARRAYS

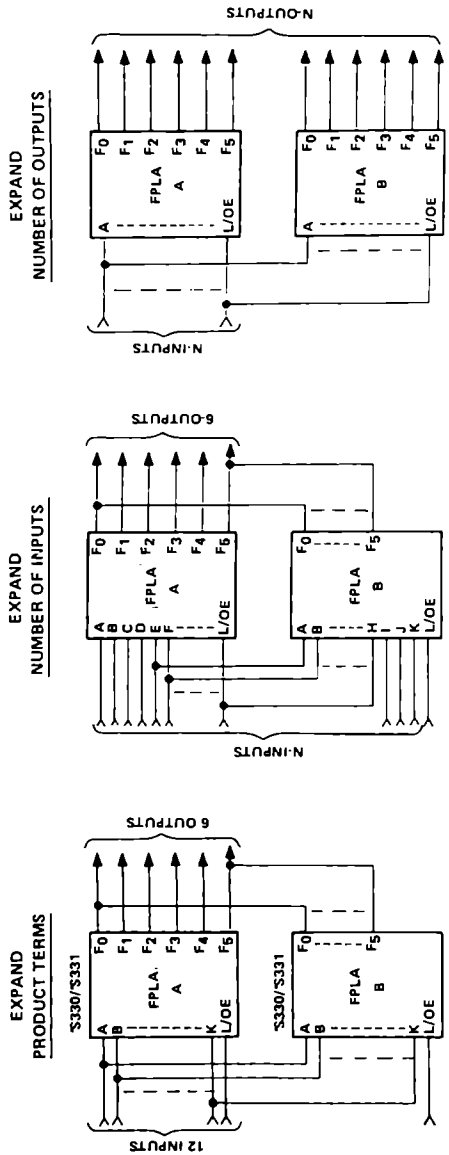
EXPAND PRODUCT TERMS
'S330/'S331
12 INPUTS
6 OUTPUTS
FPLA A
FPLA B
OVERLAP INPUTS AND OUTPUTS 1:1
• CODE OUTPUT ENABLES TO ENABLE FPLA "A" FOR SOME INPUT PATTERNS AND FPLA "B" FOR THE REST.
EXPAND NUMBER OF INPUTS
N-INPUTS
6-OUTPUTS
OVERLAP INPUTS N:N AND OUTPUTS 1:1
• OVERLAP INPUTS BY N-BITS
• CODE OUTPUT ENABLES TO ENABLE FPLA "A" OR "B" AS APPROPRIATE.
EXPAND NUMBER OF OUTPUTS
N-OUTPUTS
OVERLAP INPUTS N:N
• USE OUTPUTS INDEPENDANTLY.
• CODE OUTPUTS ENABLED FOR BOTH FPLA "A" AND "B".

FIGURE 5 – EXPANDING THE 'S330, 'S331 FPLA

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APPLICATIONS

The FPLA is efficiently suited for generating the sum of product terms which are normally required to implement:

- Memory mapping/supplemental functions
- Random logic or function generators
- Sequential controllers
- Status decoders or result interpreters
- Priority encoders

In addition, the FPLA introduces an alternative approach to the implementation of some code converters, pattern generators, and look-up tables which have commonly utilized PROMs and/or ROMs.

MEMORY CONTROL/SUPPLEMENTAL FUNCTIONS

The FPLA is ideally suited for implementing a wide variety of functions with respect to the control and/or supplementing of system memory capabilities. Some are:

- Memory mapping
- Microprogram control
- Memory patch
- PROM extension

The wide input capability of the 'S330/'S331 FPLA makes it ideal for decoding either a current memory address or a variety of status lines and generate a unique system control function.

MEMORY MAPPING/MICROPROGRAM CONTROL (See Figure 6)

These similar control functions utilize FPLAs which decode the assigned (mapped) addresses to accomplish system memory management; and/or, the FPLAs decode the current system address/status and implement the hardwired jump, branch-to-subroutine, or starting address in the microprogram control memory.

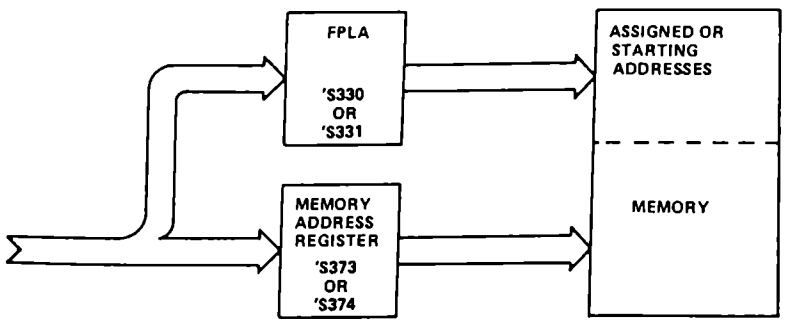

FIGURE 6 – MEMORY MAPPING/MICROPROGRAM CONTROL

MEMORY PATCH/PROM EXTENSION (See Figures 7 and 8)

These supplemental functions are cost-effective solutions for enhancing or upgrading existing memory systems or designs. Either the patch or extension can be used to correct existing deficiencies, to prioritize improved control over existing functions, or to extend the existing capabilities. Priority and source select can be programmed into the FPLA.

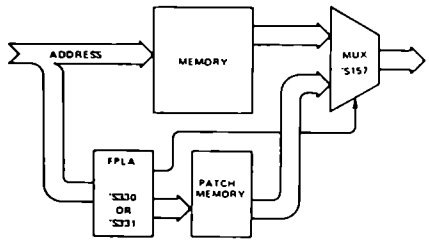

FIGURE 7 – MEMORY PATCH

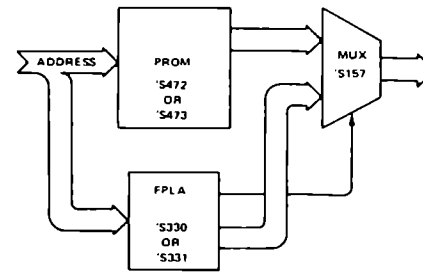

FIGURE 8 – PROM EXTENSION

DIGITAL SEQUENTIAL CONTROLLERS (See Figure 9)

This broad category of functions range from simple stand-alone machine controllers to the microprogram sequencing of any size computer or machine. The identifiable common denominator being that a sequential controller decodes a present state and generates the next state. Contrasted to a data processor or computer which generates information from operating on a word of data, the sequential controller generates information on a bit-by-bit basis.

Sequences generated can range from simple counting schemes to arbitrary bit-by-bit generation of any unique output states.

This application shows how the FPLA can simplify the implementation of a sequential controller. When the combinatorial logic of the FPLA is combined with the flexibility and synchronization of standard flip-flops in a feed-back loop, the full capability to generate a next state functional directive can be decoded from the present state: the outputs of the flip flops (present state) in conjunction with the status inputs.

STATUS DECODERS/RESULT INTERPRETERS

This broad category of functions, generally described as the elements which monitor the execution results of present instructions in sequential machines, can provide the decision-making hardware needed to both determine that the present operation is complete and simultaneously generate the next starting address or state. The actual configuration varies widely, but one popular method is to configure the FPLA similar to that shown for memory mapping.

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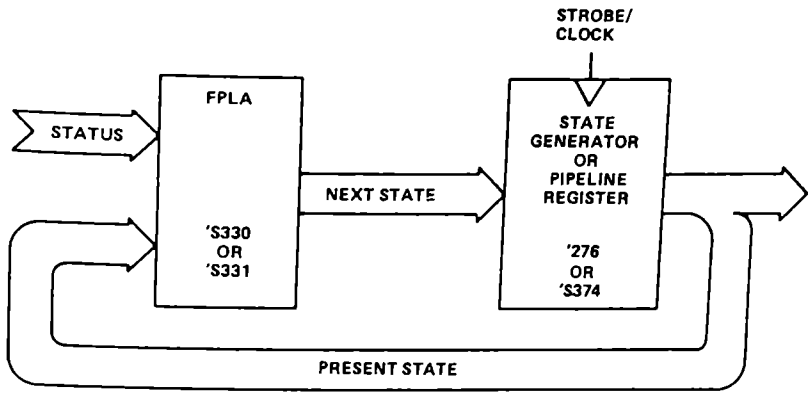


FIGURE 9 – SEQUENTIAL CONTROLLER

PRIORITY ENCODERS

The unique properties of the FPLA's capability to be programmed for decoding a number of product terms in virtaully any combination provides the user with the flexibility of identifying and implementing virtually any prioritized scheme. This option is normally available in any use shown for the 'S330/'S331.

RANDOM LOGIC OR FUNCTION GENERATORS

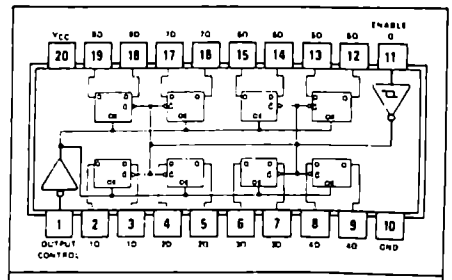
The 'S330/'S331 FPLAs provide the system designer with the options of reducing package count and/or system design time. Random gate logic can potentially be replaced at a package ratio of 12.5-to-1 up to 50-to-1 depending on the particular system needs. Function generators can be programmed directly into the FPLA from simple truth tables. In addition to reducing design and production start-up time, this technique can reduce the direct and indirect costs associated with logic and package minimization processes.

TYPES SN54S373, SN54S374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

BULLETIN NO. DL-S 7512350, OCTOBER 1975

- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading and Reloading
- Buffered Control Inputs
- Clock/Enable Input has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines
- Operates with outputs Enabled or at High Z

SN54S373 . . . J PACKAGE
SN74S373 . . . J OR N PACKAGE
(TOP VIEW)

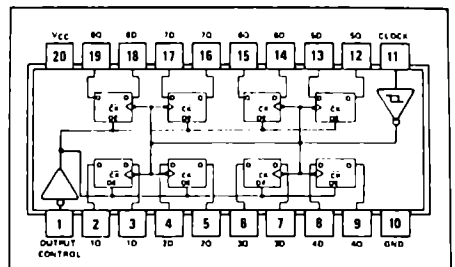


logic: see function table

SN74S373

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Hi-Z

SN54S374 . . . J PACKAGE
SN74S374 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

SN74S374

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Hi-Z

Q_0 = the level of Q before the indicated steady-state input conditions were established.
H = high level
L = low level
Hi-Z = high impedance
X = irrelevant
↑ = transition from low to high level

description

These 8-bit registers feature totem-pole 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing:

Buffer Registers

I/O Ports

Bidirectional Bus Drivers

Working Registers.

The SN54S373 and SN74S373 are transparent D-type latches meaning that while the enable (G) is high the Q output will follow the data (D) input. When the enable is taken low the output will be latched at the data that was setup.

TENTATIVE DATA SHEET
This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

description (continued)

The SN54S374 and SN74S374 are edge-triggered D-type flip-flops. On the positive transition of the clock the Q output will be set to the logic state that was setup at the D input.

Schmitt-trigger buffered inputs at the enable ('S373) and clock ('S374) lines simplifies system design as a-c and d-c noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state (Hi-Z). In the Hi-Z state the outputs neither load nor drive the bus line significantly.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S373, SN54S374 . . . . . −55°C to 125°C
SN74S373, SN74S374 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S373, SN54S374			SN74S373, SN74S374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−2			−6.5	mA
Width of clock/enable pulse, t_w	High	6			6			ns
	Low	7.3			7.3			
Data setup time, t_{su}	'S373	0↓			0↓			ns
	'S374	5↑			5↑			
Data hold time, t_h	'S373	10↓			10↓			ns
	'S374	2↑			2↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	SN54S'	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.4		V
		SN74S'	V_{IL} = 0.8 V,	I_{OH} = MAX	2.4	3.1		
V_{OL}	Low-level output voltage		V_{CC} = MIN,	V_{IH} = 2 V,			0.5	V
			V_{IL} = 0.8 V,	I_{OL} = 20 mA				
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX,	V_{IH} = 2 V,			50	μA
			V_O = 2.4 V					
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX,	V_{IH} = 2 V,			−50	μA
			V_O = 0.5 V					
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			50	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V			−250	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX	'S373		105	160	mA
				'S374		90	140	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

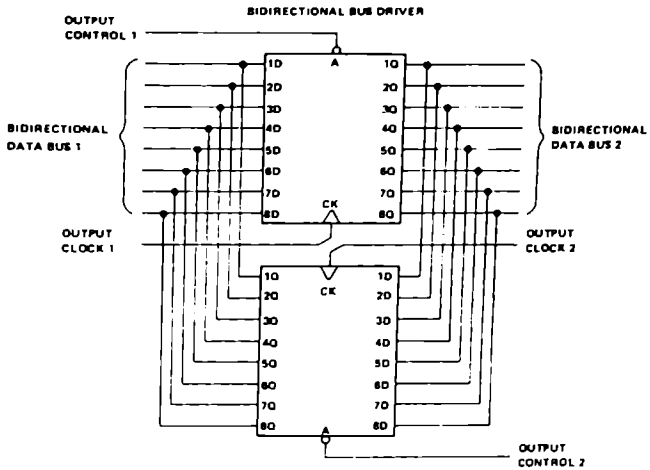
switching characteristics, V_{CC} = 5 V, T_A = 25°C

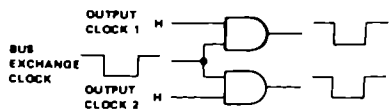
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373			'S374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Note				75	100		MHz
t_{PLH}	Data	Any Q			5	9				ns
t_{PHL}					9	13				
t_{PLH}	Clock or enable	Any Q			7	14		8	15	ns
					12	18		11	17	
t_{ZH}	Output Control	Any Q			8	15		8	15	ns
t_{ZL}					11	18		11	18	
t_{HZ}	Output Control	Any Q	C_L = 5 pF, R_L = 280 Ω, See Note		6	9		5	9	ns
t_{LZ}					8	12		7	12	

NOTE: f_{max} is tested with all outputs loaded.

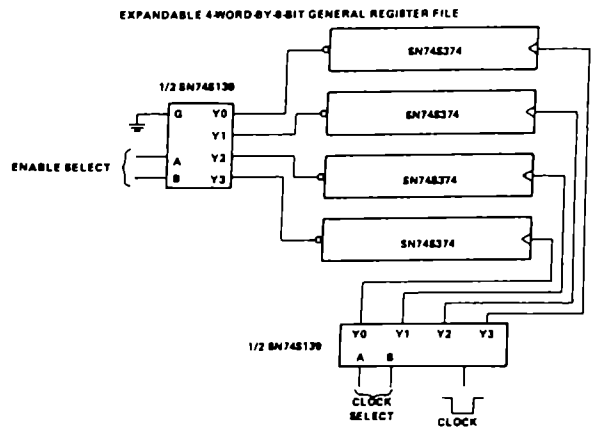
f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high level
t_{PHL} = propagation delay time, high-to-low level
t_{ZH} = output enable time to high level
t_{ZL} = output enable time to low level
t_{HZ} = output disable time from high level
t_{LZ} = output disable time from low level

APPLICATIONS





CLOCK CIRCUIT FOR BUS EXCHANGE



It cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.
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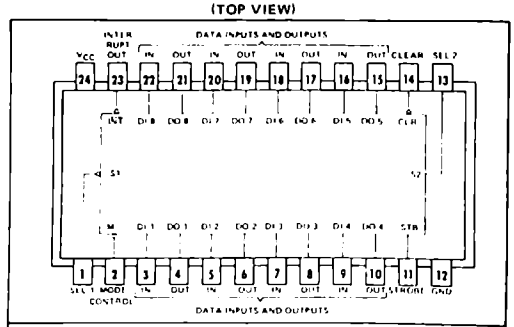
TYPES SN54S412, SN74S412 (TIM8212)
MULTI-MODE BUFFERED LATCHES

BULLETIN NO. DL S 7512351, OCTOBER 1975

- P-N-P Inputs and 3-State Outputs Maximize I/O and Data Bus Capabilities
- Data Latch Transparency Permits Asynchronous or Latched Receiver Modes
- Mode and Select Inputs Permit Storing With Outputs Enabled or Disabled
- Strobe-Controlled Flag Flip-Flop Indicates Status or Interrupt
- Asynchronous Clear Sets All Eight Data Lines Low and Initializes Status Flag
- High-Level Output Voltage, Typically 4 V, Drives Most MOS Functions Directly
- Direct Replacement for Intel 3212 or 8212

SN54S412 . . . J PACKAGE
SN74S412 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The three-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides package busy or request interrupt commands. The outputs, with a 4-volt typical high-level voltage, are compatible for driving low-threshold MOS directly.

DATA LATCHES

The eight data latches are fully transparent when the internal gate enable, G, input is high and the outputs are enabled (OE = H). Latch transparency is selected by the mode control (M), select ($\overline{S1}$ and S2), and the strobe (STB) inputs and during transparency each data output (DO_i) follows its respective data input (DI_i). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches. See data latches function table.

MODE SELECTION

An input mode or an output mode is selectable from this single input line. In the input mode, MD = L, the eight data latch inputs are enabled when the strobe is high regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken low, the latches will store the most-recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S1}$ and S2) inputs. See data latches function table.

STATUS FLIP-FLOP

The status flip-flop provides a low-level output signal when:

a. the package is selected

b. a strobe input is received.

This status signal can be used to indicate that the register is busy or to initiate an interrupt type command.

TENTATIVE DATA SHEET
This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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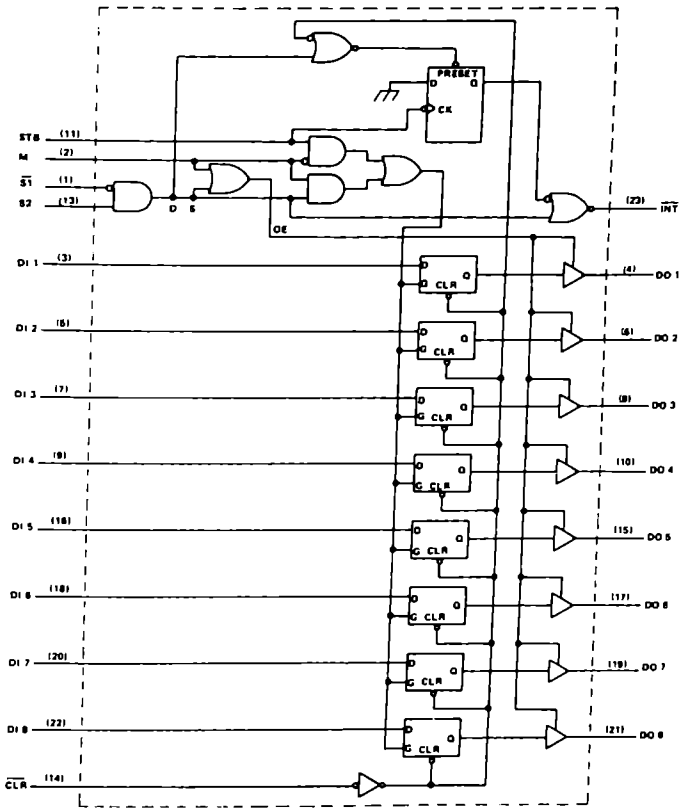
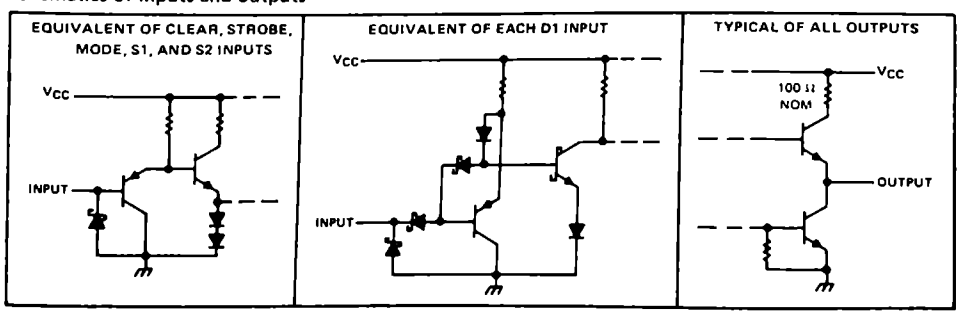
functional block diagram



schematics of inputs and outputs



DATA LATCHES FUNCTION TABLE

FUNCTION	CLEAR	M	$\overline{S1}$	S2	STB	DATA IN	DATA OUT
Clear	L	H	H	X	X	X	L
	L	L	L	H	L	X	L
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	O_O
	H	L	L	H	L	X	O_O
Data Bus	H	H	L	H	X	L	L
	H	H	L	H	X	H	H
Data Bus	H	L	L	H	H	L	L
	H	L	L	H	H	H	H

STATUS FLIP-FLOP FUNCTION TABLE

CLEAR	$\overline{S1}$	S2	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	L	H	X	L

H ≡ high level (steady state)
L ≡ low level (steady state)
X ≡ irrelevant (any input, including transitions)
Z ≡ high impedance (off)
↓ ≡ transition from low to high level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range. SN54S412 . . . . . −55°C to 125°C
SN74S412 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S412			SN74S412			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Pulse width, t_w (see Figures 1, 2, and 4)	STB or $\overline{S1}$ · S2	25			25			ns
	Clear low	25			25			
Setup time, t_{su} (see Figure 3)		15↓			15↓			ns
Hold time, t_h (see Figures 1 and 3)		20↓			20↓			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S412 MIN	SN54S412 TYP‡	SN54S412 MAX	SN74S412 MIN	SN74S412 TYP‡	SN74S412 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.85			0.85	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA		3.65	4		3.65	4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 15 mA			0.45			0.45	V
				I_{OL} = 20 mA			0.5			0.5	
I_{OZH}	Off-state output current, high-level voltage applied	DO 1 thru DO 8	V_{CC} = MAX, V_O = 2.4 V				50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	DO 1 thru DO 8	V_{CC} = MAX, V_O = 0.5 V				−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 5.25 V				20			10	μA
I_{IL}	Low-level input current	$\overline{S1}$	V_{CC} = MAX, V_I = 0.4 V				−1			−1	mA
		M					−0.75			−0.75	
		All others					−0.25			−0.25	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−65	−20		−65	mA
I_{CC}	Supply current		V_{CC} = MAX, see Note 2			82			82	130	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open, clear input at 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	STB, $\overline{S1}$, or S2	Any DO	1	C_L = 30 pF		18	27	ns
t_{PHL}						15	25	
t_{PHL}	$\overline{CLR}$	Any DO	2			18	27	ns
t_{PLH}	DI_i	DO_i	3			12	20	ns
t_{PHL}						10	20	
t_{PLH}	$\overline{S1}$ or S2	$\overline{INT}$	4	C_L = 30 pF		12	20	ns
t_{PHL}	STB	$\overline{INT}$	4			16	25	
t_{ZH}	$\overline{S1}$, S2, or M	Any DO	5	C_L = 30 pF		21	35	ns
t_{ZL}						25	40	
t_{HZ}	$\overline{S1}$, S2, or M	Any DO	5	C_L = 5 pF		9	20	ns
t_{LZ}						12	20	

t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{ZH} = output enable time to high level
t_{ZL} = output enable time to low level
t_{HZ} = output disable time from high level
t_{LZ} = output disable time from low level

PARAMETER MEASUREMENT INFORMATION

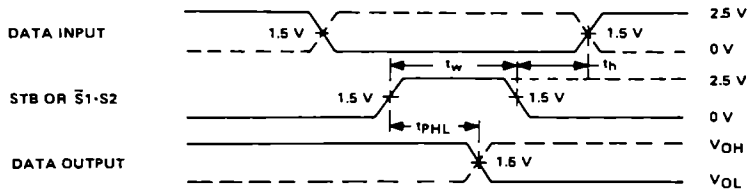


FIGURE 1 – STROBE OR SELECT TO DATA OUTPUT

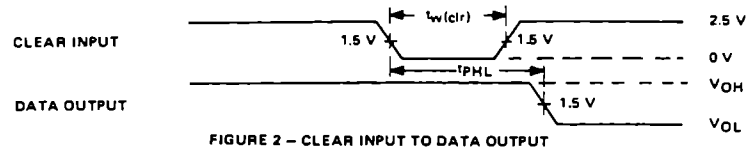


FIGURE 2 – CLEAR INPUT TO DATA OUTPUT

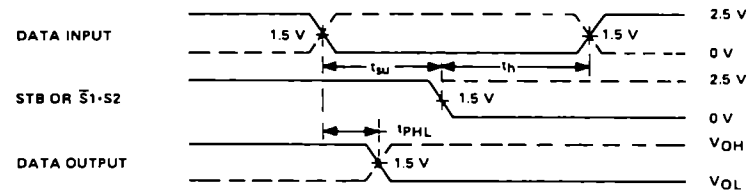


FIGURE 3 – DATA INPUT TO DATA OUTPUT

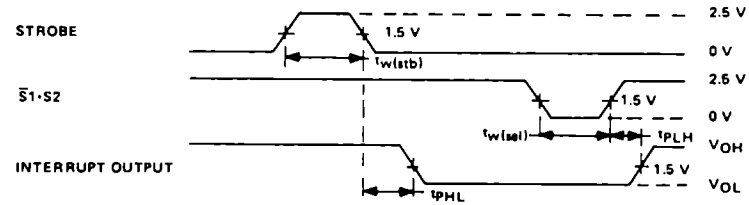


FIGURE 4 – STROBE OR SELECT TO INTERRUPT OUTPUT

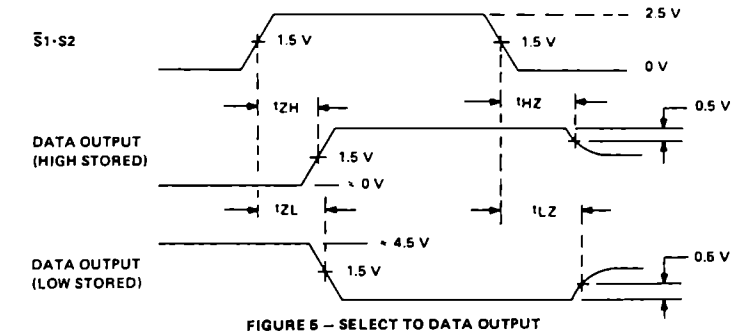


FIGURE 5 – SELECT TO DATA OUTPUT

TYPES SN74S428(TIM8228), SN74S438(TIM8238)
CONTROLLER AND BUS DRIVER FOR 8080A SYSTEMS

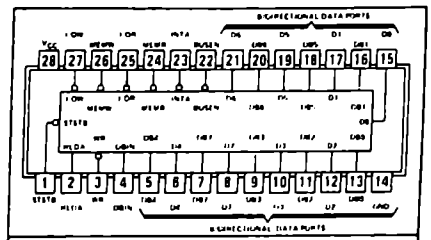
BULLETIN NO. DL S 7612488, OCTOBER 1976

- Designed to Be Interchangeable with Intel 8228 and 8238

PIN DESIGNATIONS

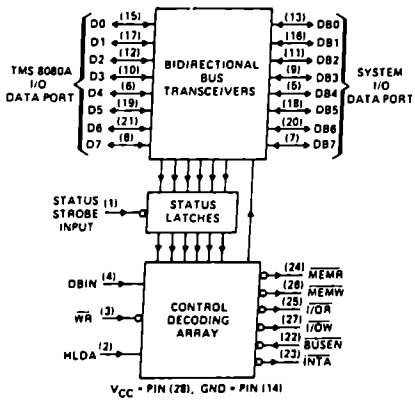
DESIGNATION	PIN NOS.	FUNCTION
D0 thru D7	15, 17, 12, 10, 6, 19, 21, 8	BIDIRECTIONAL DATA PORT (TO TMS 8080A)
DB0 thru DB7	13, 16, 11, 9, 5, 18, 20, 7	BIDIRECTIONAL DATA PORT (TO SYSTEM BUS)
$\overline{I/OR}$	25	READ OUTPUT TO I/O (ACTIVE LOW)
$\overline{IO/W}$	27	WRITE OUTPUT TO I/O (ACTIVE LOW)
$\overline{MEMR}$	24	READ OUTPUT TO MEMORY (ACTIVE LOW)
$\overline{MEMW}$	26	WRITE OUTPUT TO MEMORY (ACTIVE LOW)
DBIN	4	INPUT TO INDICATE TMS 8080A IS IN INPUT MODE (ACTIVE HIGH)
$\overline{INTA}$	23	INTERRUPT ACKNOWLEDGE OUTPUT (ACTIVE LOW)
HLDA	2	HOLD ACKNOWLEDGE INPUT (ACTIVE HIGH) FROM TMS 8080A
$\overline{WR}$	3	INPUT TO INDICATE TMS 8080A IS IN WRITE MODE (ACTIVE LOW)
$\overline{BUSEN}$	22	SYSTEM DATA PORT ENABLE INPUT (ACTIVE LOW)
$\overline{STSTB}$	1	SYNCHRONIZING STATUS STROBE INPUT FROM SN74LS424 (TIM8224)
V_{CC}	28	SUPPLY VOLTAGE (5 V)
GND	14	GROUND

N PACKAGE
(TOP VIEW)



logic: see description

functional block diagram



description

These monolithic Schottky-clamped TTL system controllers are designed specifically to provide bus-driving and peripheral-control capabilities for interfacing memory and I/O devices with the 8080A in small to medium-large microcomputer systems.

A bidirectional eight-bit parallel bus driver is provided that isolates the 8080A bus from the memory and I/O data bus allowing the system designed to utilize cost-effective memory and peripheral devices while obtaining the maximum efficiency from the microprocessor. The TTL system drivers also provide increased fan-out with a lower impedance that enhances noise margins on the system bus.

Implementation of the status latches and control decoding array of the SN74S428/SN74S438 provides for using either a single-level interrupt vector RST7 for small systems, or multiple-byte call instructions for systems needing unlimited interrupt levels.

description (continued)

With respect to the system clocks, the SN74S438 is configured to generate an advanced response for I/O or memory write output signals to further simplify peripheral control implementation of complex systems. See Figure 3.

8-bit parrallel bus transceiver

The 8-bit parallel bus transceiver buffers the 8080A data bus from the memory and I/O system bus by providing one port (DO through D7) to interface with the 8080A and another port (DBO through DB7) to interface with the system devices. The 8080A side of the transceiver is designed specifically to interface with the microprocessor data bus ensuring not only that the processor output drive capabilities are adequate, but also that the inputs are driven with enhanced noise margins. The system bus side features high fan-out buffers designed to drive a number of system devices simultaneously and directly. The system port is rated to sink ten milliamperes of current and to source one milliampere of current at standard low-threshold voltage levels.

Status lines from the 8080A instruction-status decoder and the system bus enable input (BUSEN) provide complete transceiver directional and enable control to ensure integrity of both the processor data and the system bus data.

status latches

During the beginning of each machine cycle, the six status latches receive status information from the 8080A data bus indicating the type of operation that will be performed. When the $\overline{\text{STSTB}}$ input goes low, the latches store the status data and generate the signals needed to enable and sequence the memory and I/O control outputs. The status words and types of machine cycles are enumerated in Table A.

TABLE A – STATUS WORDS

STATUS WORD	8080A STATUS OUTPUT								TYPE OF MACHINE CYCLE	'S428/'S438 COMMAND GENERATED
	D0	D1	D2	D3	D4	D5	D6	D7		
1	L	H	L	L	L	H	L	H	Instruction fetch	$\overline{\text{MEMR}}$
2	L	H	L	L	L	L	L	H	Memory read	$\overline{\text{MEMR}}$
3	L	L	L	L	L	L	L	L	Memory write	$\overline{\text{MEMW}}$
4	L	H	H	L	L	L	L	H	Stack read	$\overline{\text{MEMR}}$
5	L	L	H	L	L	L	L	L	Stack write	$\overline{\text{MEMW}}$
6	L	H	L	L	L	L	H	L	Input read	$\overline{\text{I/OR}}$
7	L	L	L	L	H	L	L	L	Output write	$\overline{\text{I/OW}}$
8	H	H	L	L	L	H	L	L	Interrupt acknowledge	$\overline{\text{INTA}}$
9	L	H	L	H	L	L	L	H	Halt acknowledge	NONE
10	H	H	L	H	L	H	L	L	Interrupt acknowledge at halt	$\overline{\text{INTA}}$
	INTA	$\overline{\text{WO}}$	STACK	HLTA	OUT	M1	INP	MEMR	STATUS INFORMATION	

decoding array

The decoding array receives enabling commands from the status latches and sequencing commands from the 8080A and generates memory and I/O read/write commands and an interrupt acknowledgement.

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description (continued)

The read commands ($\overline{MEMR}$, $\overline{I/OR}$) and the interrupt acknowledgement ($\overline{INTA}$) are derived from the status bit(s) and the data bus input mode (DBIN) signal. The write commands ($\overline{MEMW}$, $\overline{I/OW}$) are derived from the status bit(s) and the write mode ($\overline{WR}$) signal. (See Table A.) All control commands are active low to simplify interfacing with memory and I/O controllers.

The interrupt acknowledgement ($\overline{INTA}$) command output is actually a dual function pin. As an output, its function is to provide the $\overline{INTA}$ command to the memory and I/O peripherals as decoded from the status inputs and latches. When CALL is used as an interrupt instruction, the SN74S428/SN74S428 generates the proper sequence of control signals. Additionally, the terminal includes high-threshold decoding logic that permits it to be biased through a one-kilohm series resistor to the 12-volt supply to implement an interrupt structure that automatically inserts an RST7 instruction on the bus when the DBIN input is active and an interrupt is acknowledged. This capability provides a single-level interrupt vector with minimal hardware.

The asynchronous bus enable ($\overline{BUSEN}$) input to the decoding array is a control signal that protects the system bus. The system bus can be accessed and driven from the SN74S428/SN74S428 controller only when the $\overline{BUSEN}$ input is at a low voltage level.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	D0 thru D7			−10	μA
	All others			−1	mA
Low-level output current, I_{OL}	D0 thru D7			2	mA
	All others			10	
Status strobe pulse width, $t_{w(STSTB)}$ (see Figure 3)		22			ns
Setup time, t_{su} (see Figure 3)	Status inputs D0 thru D7	8			ns
	System bus inputs to HLDA	10			
Hold time, t_h (see Figure 3)	Status inputs D0 thru D7	5			ns
	System bus inputs to HLDA	20			
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −5 mA			−1	V
V_{OH}	High-level output voltage	D0 thru D7	V_{CC} = MIN,	V_{IH} = 2 V,	3.6	4		V
		All other outputs	V_{IL} = 0.8 V,	I_{OH} = MAX	2.4			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.45	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX,	V_O = 5.25 V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX,	V_O = 0.45 V			−100	μA
I_{IH}	High-level input current	$\overline{INTA}$	V_{CC} = MIN,	See Figure 1			5	mA
		D0 thru D7	V_{CC} = MAX,	V_I = 5.25 V			20	μA
		All other inputs					100	
I_{IL}	Low-level input current	D2 or D6	V_{CC} = MAX,	V_I = 0.45 V			−750	μA
		$\overline{STSTB}$					−500	
		All other inputs					−250	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−15		−90	mA
I_{CC}	Supply current		V_{CC} = MAX			140	190	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see figure 3

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PD}	D0 thru D7	DB0 thru DB7	C_L = 100 pF,	See Figure 2	5		40	ns
t_{PD}	DB0 thru DB7	D0 thru D7	C_L = 25 pF,	See Figure 2			30	ns
t_{PHL}	$\overline{STSTB}$	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$, $\overline{I/OW}$, $\overline{MEMW}$	C_L = 100 pF,	See Figure 2	20		60	ns
t_{PD}	$\overline{WR}$	$\overline{I/OW}$, $\overline{MEMW}$			5		45	ns
t_{PLH}	DBIN	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$					30	ns
t_{PLH}	HLDA	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$					25	ns
t_{PZX}	DBIN	D0 thru D7	C_L = 25 pF,	See Figure 2			45	ns
t_{PXZ}	DBIN	D0 thru D7					45	ns
t_{PZX}	$\overline{STSTB}$, $\overline{BUSEN}$	DB0 thru DB7	C_L = 100 pF,	See Figure 2			30	ns
t_{PXZ}	$\overline{BUSEN}$	DB0 thru DB7					30	ns

¶ t_{PD} = propagation delay time
t_{PHL} = propagation delay time, high-to-low-level output
t_{PLH} = propagation delay time, low-to-high-level output
t_{PZX} = output enable time from high-impedance state
t_{PXZ} = output disable time to high-impedance state

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PARAMETER MEASUREMENT INFORMATION

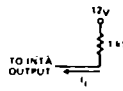


FIGURE 1–$\overline{\text{INTA}}$ INPUT CURRENT TEST CIRCUIT

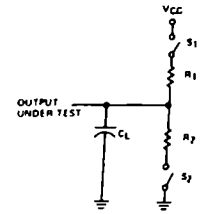
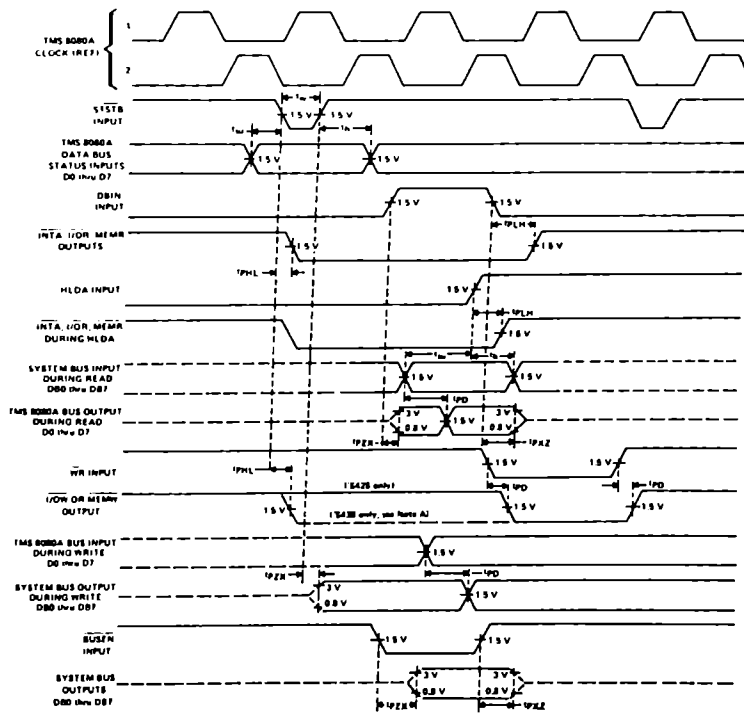


FIGURE 2–SWITCHING CHARACTERISTICS LOAD CIRCUIT


TMS 8080A CLOCK (REF)
SYSTB INPUT
TMS 8080A DATA BUS STATUS INPUTS D0 thru D7
DBIN INPUT
INTA, I/OR, MEMR OUTPUTS
HLDA INPUT
INTA, I/OR, MEMR DURING HLDA
SYSTEM BUS INPUT DURING READ D80 thru D87
TMS 8080A BUS OUTPUT DURING READ D0 thru D7
WR INPUT
I/OW OR MEMW OUTPUT
TMS 8080A BUS INPUT DURING WRITE D0 thru D7
SYSTEM BUS OUTPUT DURING WRITE D80 thru D87
BUSEN INPUT
SYSTEM BUS OUTPUTS D80 thru D87
1.5 V
3 V
0.8 V

NOTE A: Advanced response of $\overline{\text{I/OW}}$ or $\overline{\text{MEMW}}$ for the SN74S438 is indicated by the dashed line.

FIGURE 3–VOLTAGE WAVEFORMS

TYPICAL APPLICATION DATA

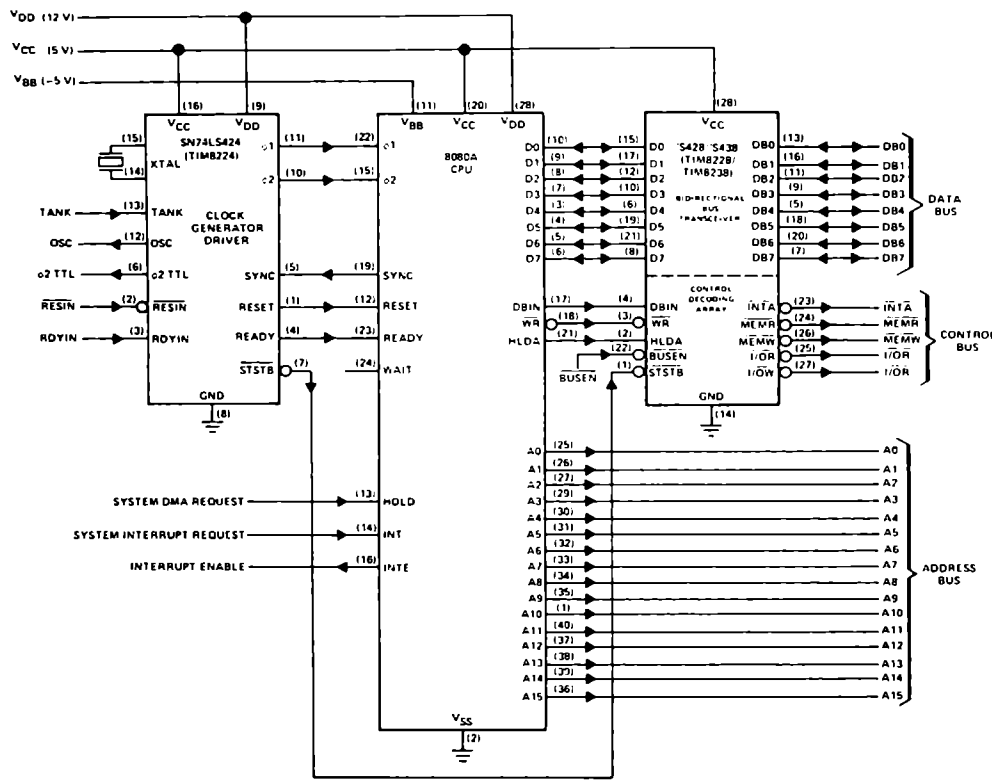


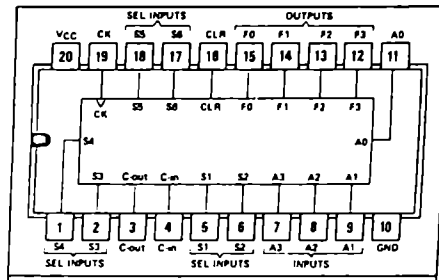
FIGURE 4–SYSTEM INTERFACING WITH CENTRAL PROCESSING UNIT

TYPES SN54S482, SN74S482
4-BIT-SLICE EXPANDABLE CONTROL ELEMENTS

BULLETIN NO. DL-S 7612384, MARCH 1976

- 4-Bit Slice is Cascadable to N-Bits
- Designed Specifically for Microcontroller/ Next-Address Generator Functions
- Increment/Decrement by One (Immediate or Direct Symbolic Addressing Modes)
- Offset, Vector, or Branch (Indexed or Relative Addressing Modes)
- Store Up to Four Returns or Links (Program Return Address from Subroutine)
- Program Start or Initialize (Return to Zero or Clear Mode)
- On-Chip Edge-Triggered Output Register (Provides Steady-State Micro-Address/ Instruction)
- High-Density 20-Pin Dual-in-Line Package with 300-Mil Row Pin Spacing

SN54S482 . . . J PACKAGE
SN74S482 . . . J OR N PACKAGE
(TOP VIEW)



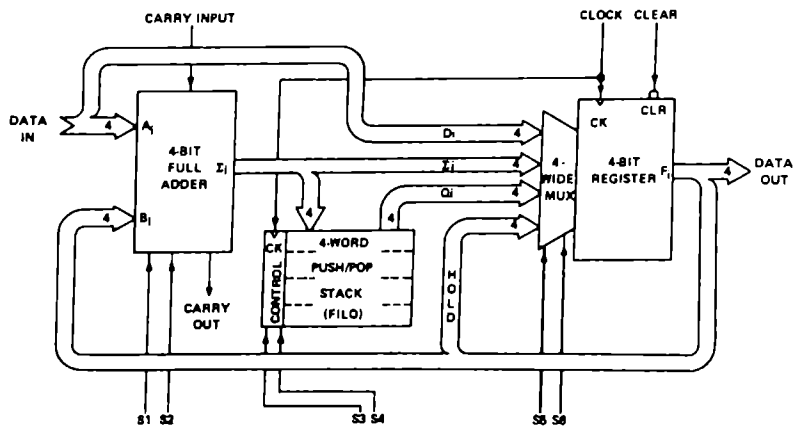
positive logic: See function table.

description

The 'S482 is a high-performance Schottky TTL 4-bit-slice control element for use in any computer/control application requiring the coupling of high-performance bipolar speeds with the flexibility of microprogram control and bit-slice expandability. When used as a next-address generator, two 'S482 elements can address up to 256 words of microprogram; three elements can addresss up to 4096 words of microprogram; or a number of 'S482 elements can generate N words in multiples of four lines.

Comprised of an output register, push-pop stack, and a full adder, the 'S482 provides the capability to implement multiway testing needed to generate or to determine and select the source of the next function of microprogram address.

functional block diagram



This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

output register and source functions

The 4-bit edge-triggered register provides a steady-state output throughout each system clock cycle. An asynchronous clear extends the multiway testing to directly implement system initialization at ROM address zero.

Two source-select lines (S5, S6) provide the output register with access to either the current instruction (no change), an operand or address stored in the push-pop stack, the output of a four-function full adder, or a direct data-in address port. The sources and functions are summarized in Tables I and II.

TABLE I. REGISTER-SOURCE FUNCTIONS

SELECT		REGISTER INPUT SOURCE
S5	S6	
L	L	DATA-IN PORT (DI)
L	H	FULL ADDER OUTPUTS (ΣI)
H	L	PUSH-POP STACK OUTPUTS (QI)
H	H	REGISTER OUTPUTS (HOLD)

H = high level, L = low level

TABLE II. PUSH-POP STACK CONTROL AND REGISTER-SOURCE FUNCTIONS

	INPUTS						INTERNAL	OUTPUTS
	S3	S4	S5	S6	CLOCK	CLEAR	QiA	Fi
HOLD	X	X	X	X	L	H	QiA0	Fi0
CLEAR	X	X	X	X	X	L	QiA0	L
PUSH-POP STACK "HOLD"	L	L	L	L	↑	H	QiA0*	DI
	L	L	L	H	↑	H	QiA0*	ΣI
	L	L	H	L	↑	H	QiA0*	QiA0
	L	L	H	H	↑	H	QiA0*	Fi0
PUSH-POP STACK "LOAD"	L	H	L	L	↑	H	ΣI*	DI
	L	H	L	H	↑	H	ΣI*	Σi
	L	H	H	L	↑	H	ΣI*	QiA0
	L	H	H	H	↑	H	ΣI*	Fi0
PUSH-POP STACK "POP"	H	L	L	L	↑	H	QiB0†	Di
	H	L	L	H	↑	H	QiB0†	Σi
	H	L	H	L	↑	H	QiB0†	QiA0
	H	L	H	H	↑	H	QiB0†	Fi0
PUSH-POP STACK "PUSH"	H	H	L	L	↑	H	Σi‡	DI
	H	H	L	H	↑	H	Σi‡	Σi
	H	H	H	L	↑	H	Σi‡	QiA0
	H	H	H	H	↑	H	Σi‡	Fi0

MSB LSB
i = 3, 2, 1, 0
AI = Data inputs
QiA = Push-pop stack word A output (internal)
QiA0 = the level of QI before the indicated inputs conditions were established.

Fi = Device outputs
Fi0 = the level of Fi before the indicated input conditions were established.
Σi = Adder outputs (internal)
*QiB, QiC, QiD do not change
†QiD0 → QID, QiD0 → QIC, QiC0 → QIB, QIB0 → QIA
‡QiA0 → QiB, QIB0 → QiC, QiC0 → QID

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push-pop stack control

The 4-word push-pop stack can be used for nesting up to four levels of program or return (link) addresses. In the load mode, the first (top) word is filled with new data from the output of the full adder, and no push occurs meaning that previous data at that location is lost. However, all other word locations in the push-pop stack remain unchanged. In the push mode, the new word is again entered in the first (top) location; however, previous data residing in the top three words are pushed down one word location and retained at their new locations. The bottom word is written over and lost.

In the pop mode, words in the push-pop stack move up one location on each clock transition. A unique function is provided by the bottom (fourth) register as its content is retained during the pop mode, and after 3 clock transitions, all words in the stack are filled with the operand/address that occupied the bottom register.

The operand/address will remain available indefinitely if stack functions are limited to the pop or hold modes.

The push-pop stack functions are shown in Tables II and III.

TABLE III. PUSH-POP STACK FUNCTIONS

	FUNCTION	SEL. S3	SEL. S4	REG. D	REG. C	REG. B	REG. A	INPUT/ OUTPUT
BIT 0	LOAD	L	H	QiD0	QiC0	QiB0	← Σi	ΣI IN
BIT 1	PUSH	H	H	← QiC0	← QiB0	← QiA0	← ΣI	ΣI IN
BIT 2	POP	H	L	↶ → QiD0	→ QiD0	→ QiC0	→ QiB0	QiA OUT
BIT 3	HOLD	L	L	QiD0	QiC0	QiB0	QiA0	QiA OUT

†Link operations show previous data location after clock transition.

full adder

The four-function full adder is controllable from select inputs S1 and S2 to perform:

A or B incrementation, or decrementation of B

Unconditional jumps or relative offsets

No change

Return to zero or one

Incrementation can be implemented by forcing a carry (high) into the ALU. In this mode either of the following options are possible:

1. Increment (A plus zero plus carry)
2. Increment B (zero plus B plus carry), or decrement B (all highs at A then A plus B with carry input low and disregard, don't use, carry out)
3. Increment the jump or offset (A plus B plus carry)

full adder (continued)

4. Start at zero or one and increment on each clock (select zero plus zero plus carry, then select zero plus B plus carry), or set register to N and decrement B (see 2 above).
5. No change (carry input is always active and removal of carry combined with either the ALU or register hold mode will retain the current address).

Unconditional jumps can be implemented by applying and selecting the jump directly from the data inputs to the output register. Offset can be accomplished by summing the output register with the offset magnitude (A plus B) with carry low.

The ALU functions are shown in Table IV.

TABLE IV. ADDRESS CONTROL FUNCTIONS

INPUTS		INTERNAL
S1	S2	Σi
H	H	0 PLUS 0 PLUS C-in
H	L	0 PLUS Bi PLUS C-in
L	H	Ai PLUS 0 PLUS C-in
L	L	Ai PLUS Bi PLUS C-in

compound generator functions

As the function-select lines of the register sources, push-pop stack, and adder are independent, compound functions can be selected to occur on the next clock transition.

Subroutine branches and returns can be simplified by saving the return or link addresses in the push-pop stack. This branch-and-save function can be accomplished on the same clock time as follows:

DATA-IN	ADDER	PUSH-POP STACK	REGISTER SOURCE
Branch address	Zero plus B plus one (S1 = H, S2 = L)	Push (S3 = S4 = H)	Data-in (S5 = S6 = L)

Up to four branches can be made with the return stored in the 4-word push-pop stack.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S482 . . . . . −55°C to 125°C
SN74S482 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. All voltage values are with respect to network ground terminal.

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recommended operating conditions

		SN54S482			SN74S482			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Carry output			−1			−1	mA
	Any F output			−2			−2	
Low-level output current, I_{OL}	Carry output			10			10	mA
	Any F output			16			16	
Setup time, t_{su}	Data-in, S5, S6	0↑			0↑			ns
	Data-in via adder	20↑			15↑			
	S1, S2	40↑			30↑			
	S3, S4	20↑			15↑			
	Clear-inactive state	0↑			0↑			
Pulse width, t_w	Clock (high or low)	50			30			ns
	Clear (low)	15			15			
Clock input rise time, t_r				50			50	ns
Hold time, t_h	Data-in, S5, S6	30↑			25↑			ns
	Data-in via adder	15↑			10↑			
	S1, S2	15↑			10↑			
	S3, S4	25↑			20↑			
Operating free-air temperature, T_A		−55		125	0	25	70	°C

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S482			SN74S482			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	S1, S2, Cin	V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
		S3, S4, S5, S6, clock					100			100	
		Clear					250			250	
		Any A					150			150	
I_{IL}	Low-level input current	S1, S2	V_{CC} = MAX,	V_I = 0.5 V			−1			−1	mA
		C-in					−0.8			−0.8	
		S3, S4					−1.2			−1.2	
		Any A, S5, S6, CK					−2			−2	
		Clear					−4			−4	
		Clock					−2.8			−2.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−110	−40		−110	mA
I_{CC}	Supply current		V_{CC} = MAX			90	130		90	140	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	SN54S482			SN74S482			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLOCK	DATA OUT	C_L = 15 pF, R_L = 280 Ω		12	30		12	25	ns
t_{PHL}					15	30		15	25	
t_{PHL}	CLEAR	DATA OUT			12	25		12	20	ns
t_{PLH}	CARRY IN	CARRY OUT			12	22		12	18	ns
t_{PHL}					10	22		10	18	
t_{PLH}	DATA IN	CARRY OUT			17	30		17	25	ns
t_{PHL}					12	30		12	25	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

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The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

Memories/Support Functions Mechanical Data

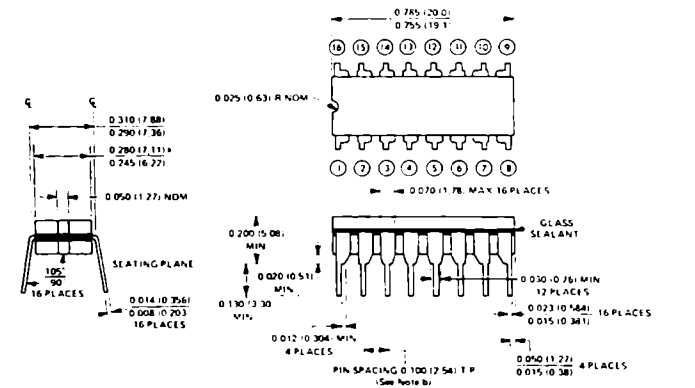
DECEMBER 1976

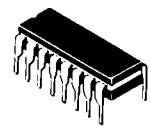
TEXAS INSTRUMENTS
INCORPORATED

J ceramic dual-in-line package

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, 20-, or 24-lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) or 0.600 (15,24) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

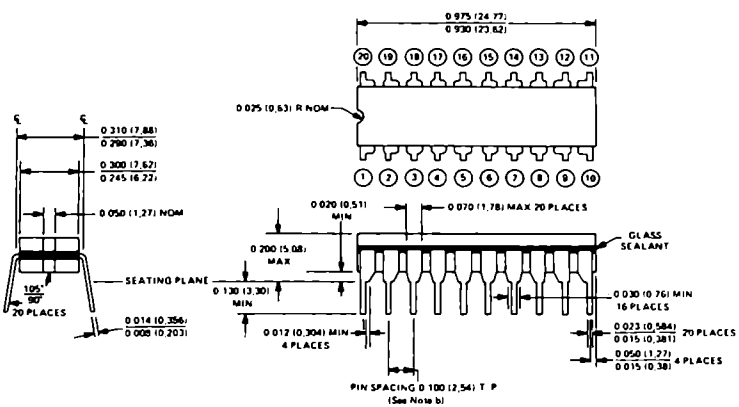
16-PIN J CERAMIC

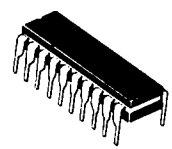




*For memories of 64 bits and up and a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, this maximum is 0.300 (7,62). All other dimensions apply without modification.

20-PIN J CERAMIC





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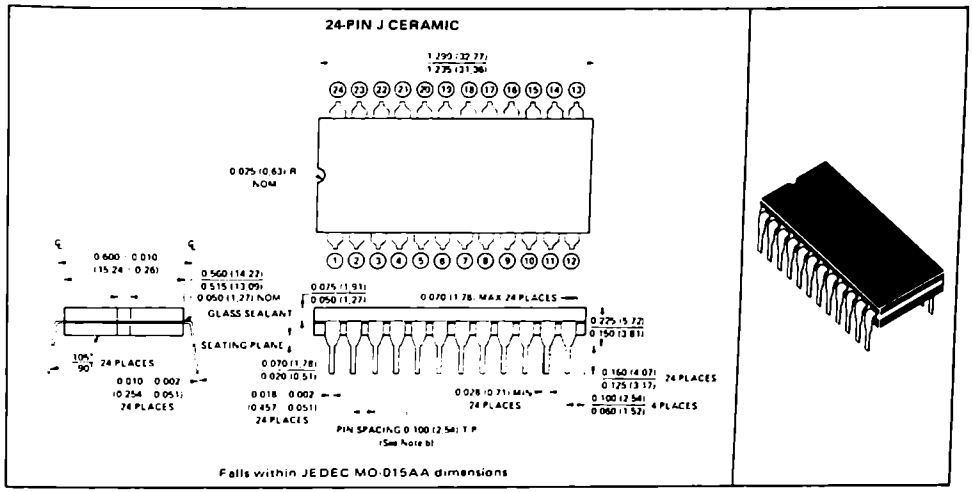
J ceramic dual-in-line packages (continued)

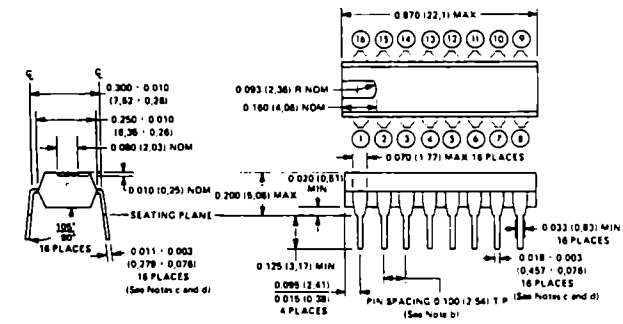


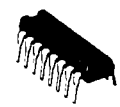
NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

N plastic dual-in-line packages

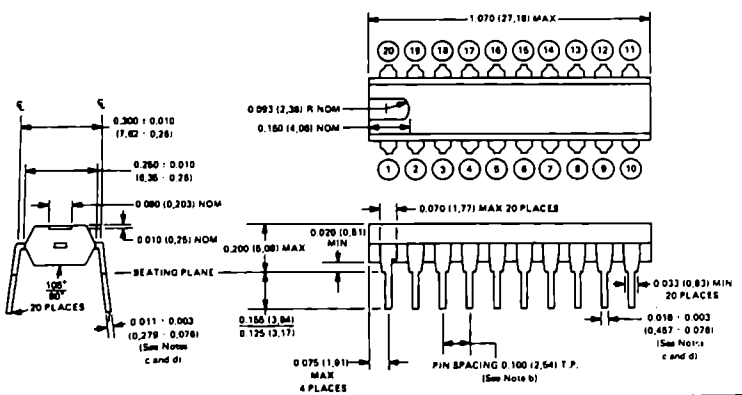
These dual-in-line packages consist of a circuit mounted on a 14-, 16-, 20-, or 28-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting hole rows on 0.300 (7,62) or 0.600 (15,24) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

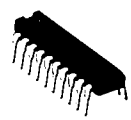
16-PIN N PLASTIC





20-PIN N PLASTIC





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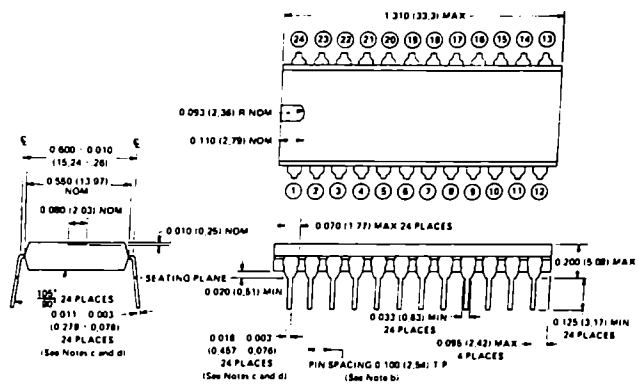
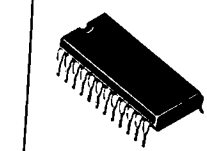
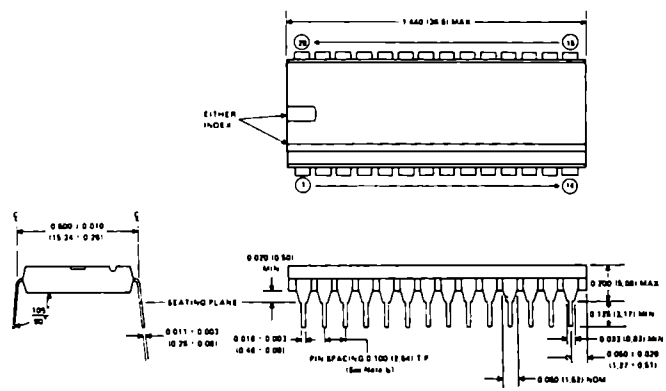
N plastic dual-in-line packages (continued)

24-PIN N PLASTIC





28-PIN N PLASTIC

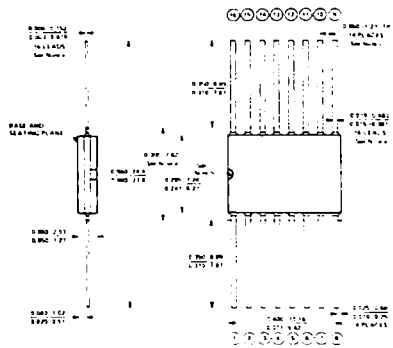


NOTES. a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 (0,50) above the seating plane.

W ceramic flat package

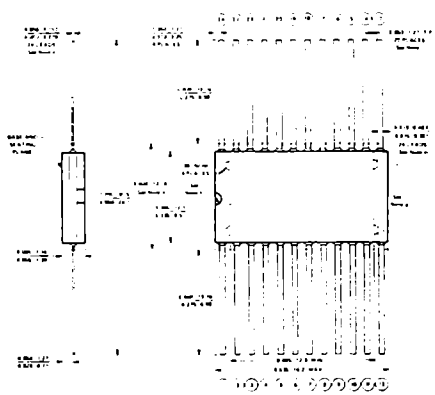
These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 14-, 16-, or 24-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

16 PIN W CERAMIC

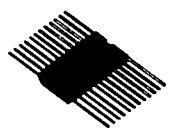


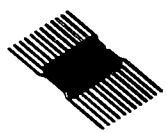
Falls within JEDEC MO-004AG Dimensions

24 PIN W CERAMIC



Falls within JEDEC MO-019AA Dimensions





NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Index point is provided on cap for terminal identification only.
c. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.
e. Not applicable for solder dipped leads.
f. When solder-dipped leads are specified, dipped area extends from lead tip to within 0.050 (1,27) of package body.
g. End configuration of 24-pin package is at the option of TI.

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